APPLICATION NOTE

# Application information for TDA8357J N2 and TDA8359J N2 deflection output circuits

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PHILIPS

**ABSTRACT**

This report gives a description of the TDA8357JN1 and the TDA8359JN1 version with a description of the TDA8357JN2 and the TDA8359JN2 version together with application aspects.

## APPLICATION NOTE

# Application information for TDA8357JN2 and TDA8359JN2 deflection output circuit

## AN01056

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**Summary**

In this report you can find an application and product description of the DC coupled deflection output circuit with the type number TDA8357J and TDA8359J. The TDA8359J is functional the same as the TDA8357J, but the TDA8359J is able to deliver a higher output current. A description is given of the differences between the TDA8357JN1 / TDA8359JN1 and TDA8357JN2 / TDA8359JN2. The application design procedure and the application investigations are given at the end of this report.

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# 1. INTRODUCTION.

The TDA8357J / TDA8359J are integrated power circuits for use in 90° and 110° colour deflection systems. They contain a vertical deflection bridge output, which operates as a high efficiency class G system and can handle field frequencies from 25 to 200 Hz. The vertical deflection coil of a 4 : 3 as well a 16 : 9 picture tube can be connected to this vertical deflection device. Due to the bridge configuration a DC deflection output application can be designed with a single positive main supply of typical 12-Volt and a positive flyback supply of typical 45-Volt. (Depending on the vertical deflection coil data). The input configuration is symmetrical in order to have improved EMI behaviour.

The integrated circuit is designed in a Low Voltage DMOS (LVDMOS) process that combines bipolar, CMOS and DMOS components. DMOS output transistors (MOSFETs) are used because of the absence of secondary breakdown, which gives a better SOAR performance. The internal circuits are designed in such way that only a few external components are needed to get a correct working application.

The TDA8359J is functional the same as the TDA8357J vertical deflection output stage. The TDA8359J differs in only one aspect from the TDA8357J; it is able to deliver a higher output current, therefor being more suitable for large picture tubes.

The TDA8357J is the successor for the TDA8356 vertical deflection output stage and the TDA8359J is the successor for the TDA8351 vertical deflection output stage. The main reason to develop successors was to reduce the voltage drop across the output stage and have a better temperature distribution.

## 1.1 Features.

- Few external components required
- High efficiency fully DC coupled vertical bridge output circuit
- Short rise and fall time of the vertical flyback switch
- Temperature (thermal) protection circuit
- Blanking pulse generator (guard)
- Improved EMC performance due to differential inputs

## 1.2 Ordering information.

| Type Number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA8357J | DBS9P | plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad | SOT523-1 |
| TDA8359J | DBS9P | plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad | SOT523-1 |

### 1.3 Block diagram

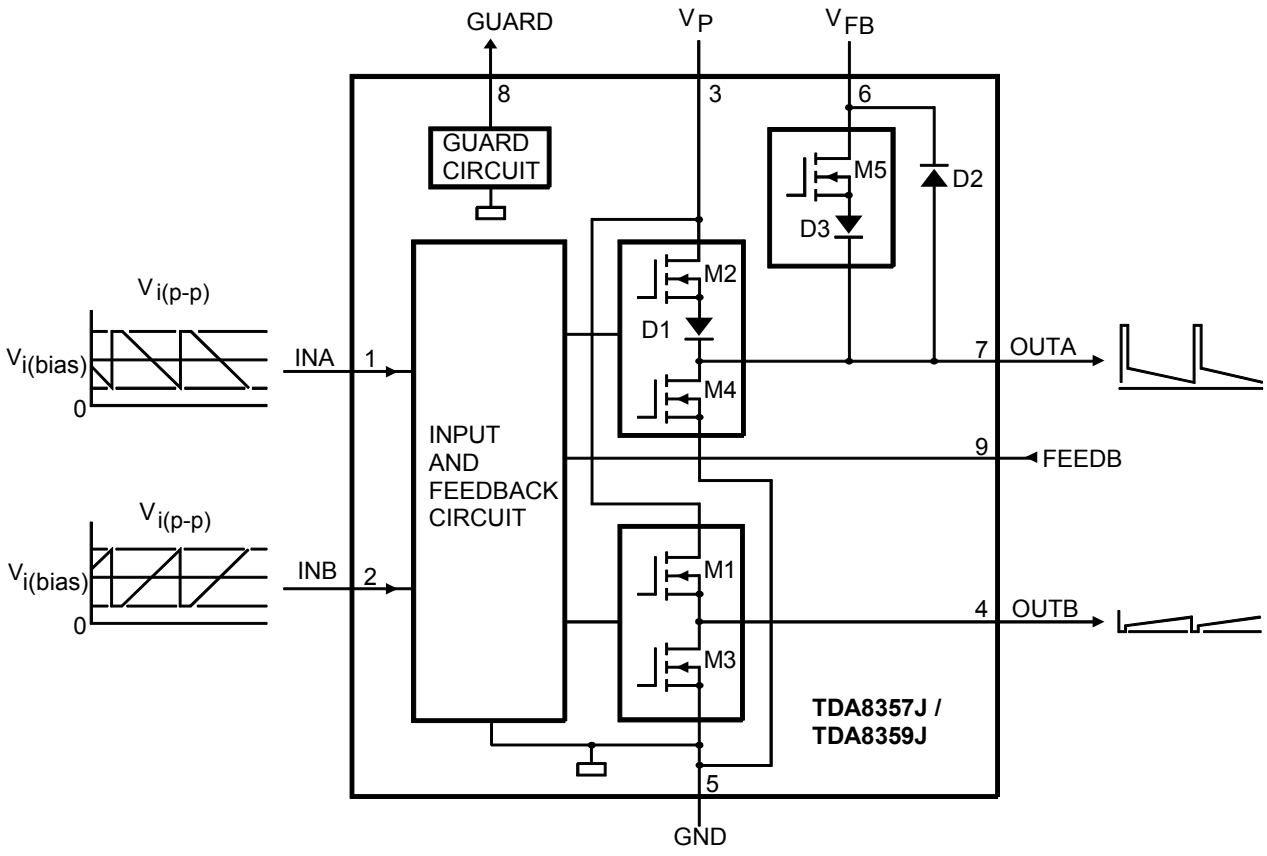
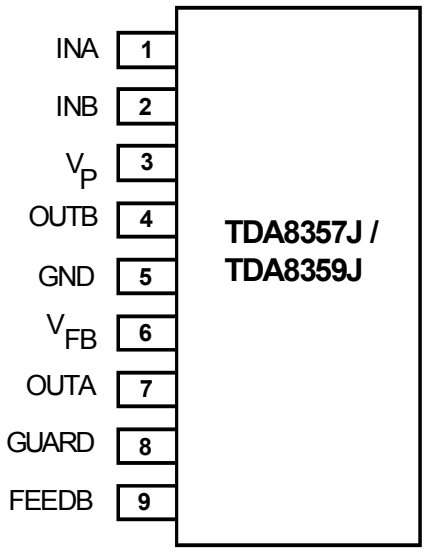



fig 1: Block diagram.

### 1.4 Pinning

| Symbol | Pin | Description |
|---|---|---|
| INA | 1 | input A |
| INB | 2 | input B |
| $V_P$ | 3 | supply voltage |
| OUTB | 4 | output B |
| GND | 5 | ground |
| $V_{FB}$ | 6 | flyback supply voltage |
| OUTA | 7 | output A |
| GUARD | 8 | guard output |
| FEEDB | 9 | feedback input |



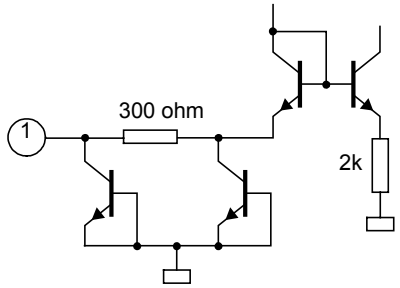
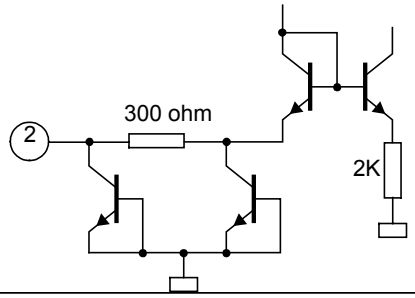
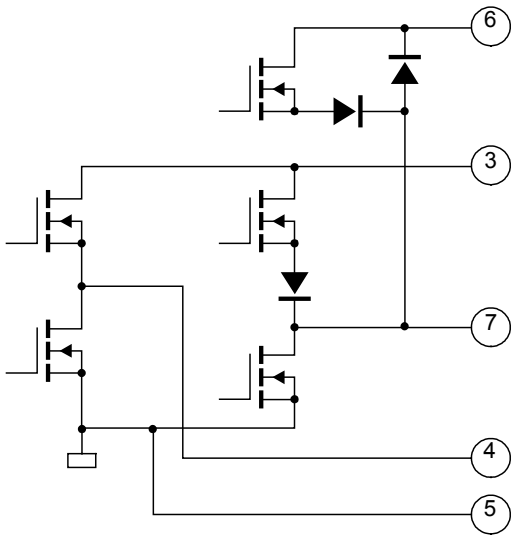

### 1.5 Quick reference data

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_P$ | supply voltage | | 7.5 | 12 | 18 | V |
| $V_{FB}$ | flyback supply voltage | | $2xV_P$ | 45 | 66 | V |
| $I_{q(P)(av)}$ | average quiescent supply current | during scan | - | 10 | 15 | mA |
| $I_{q(FB)(av)}$ | average quiescent flyback supply current | during scan | - | - | 10 | mA |
| $P_{tot}$ | **TDA8357J:** total power dissipation | | - | - | 8 | W |
| $P_{tot}$ | **TDA8359J:** total power dissipation | | - | - | 10 | W |
| **Input and outputs** | | | | | | |
| $V_{i(dif)(p-p)}$ | differential input voltage (peak-to- peak value) | | - | 1000 | 1500 | mV |
| $I_{o(p-p)}$ | **TDA8357J:** output current (peak-to-peak value) | | - | - | 2.0 | A |
| $I_{o(p-p)}$ | **TDA8359J:** output current (peak-to-peak value) | | - | - | 3.2 | A |
| **Flyback switch** | | | | | | |
| $I_{o(peak)}$ | **TDA837J:** maximum (peak) output current | $t \leq 1.5$ ms | - | - | ±1.2 | A |
| $I_{o(peak)}$ | **TDA839J:** maximum (peak) output current | $t \leq 1.5$ ms | - | - | ±1.8 | A |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Thermal data; in accordance with IEC 747-1** | | | | | | |
| $T_{stg}$ | storage temperature | | -55 | - | +150 | °C |
| $T_{amb}$ | ambient temperature | | -25 | - | + 85 | °C |
| $T_j$ | junction temperature | | - | - | +150 | °C |
| $R_{th(j-c)}$ | **TDA8357J:** thermal resistance from junction to case | | - | - | 6 | K/W |
| $R_{th(j-c)}$ | **TDA8359J:** thermal resistance from junction to case | | - | - | 3 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | - | - | 65 | K/W |

## 2. DEVICE DESCRIPTION AND APPLICATION INFORMATION

### 2.1 Internal pin configuration

| Pin | Symbol | Equivalent circuit |
|---|---|---|
| 1 | INA |  |
| 2 | INB |  |
| 3 | $V_P$ |  |
| 4 | OUTB | |
| 5 | GND | |
| 6 | $V_{FB}$ | |
| 7 | OUTA | |

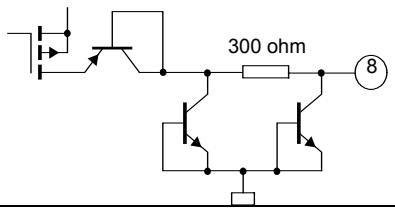
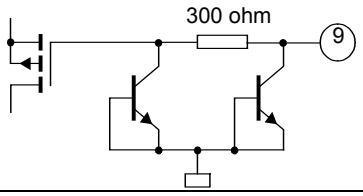
| Pin | Symbol | Equivalent circuit |
|---|---|---|
| 8 | GUARD |  |
| 9 | FEEDB |  |

fig 2: Internal circuit configuration

### 2.2 Application diagram

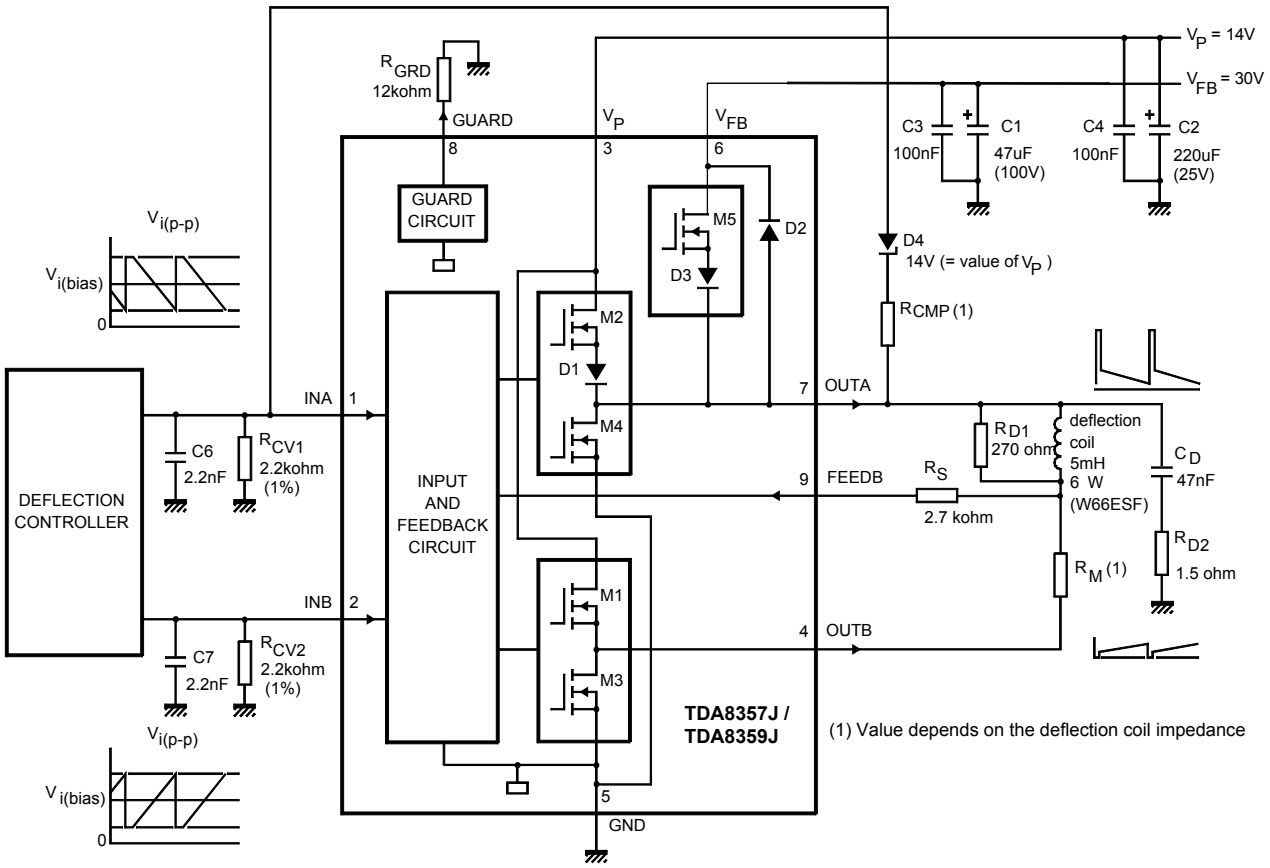



fig 3: Application diagram.

The TDA8357J / TDA8359J are vertical drive circuits in a bridge configuration. The output amplifiers are driven in opposite phase.

When looking at the application diagram, the following components can be described in short terms (detailed information is given in the succeeding sections).
The input circuits of the TDA8357J / TDA8359J are differential voltage inputs. The external resistors $R_{cv1}$ and $R_{cv2}$ convert the output currents of the TV signal processor into input voltages. The differential input voltage is compared with the voltage across the measuring resistor $R_M$ that provides feedback information. The deflection coil is connected between OUTA and resistor $R_M$ and OUTB.
The damping resistor $R_{D1}$ is connected across the deflection coil for HF loop stability. The damping resistor compensation, which consists of a resistor $R_{CMP}$ in series with a zenerdiode D4, compensates current differences in the damping resistor during scan and flyback and assures a short settling time.

### 2.3 Vertical amplifier

In many conventional deflection output circuits, the deflection coil must be AC coupled. This will require an expensive coupling capacitor of approximately 2200 µF. Beside higher costs, the coupling capacitor can cause picture bounce after switching between channels on the TV set. This capacitor can be omitted in a DC coupled deflection output circuit.

The TDA8357J / TDA8359J are DC coupled deflection output circuits, which have no bounce effect during channel switching. By using differential mode inputs the EMC immunity is improved. The deflection coil and the measuring resistor $R_M$ are connected between the output amplifiers of the TDA8357J / TDA8359J that are driven in opposite phase. See fig 3.

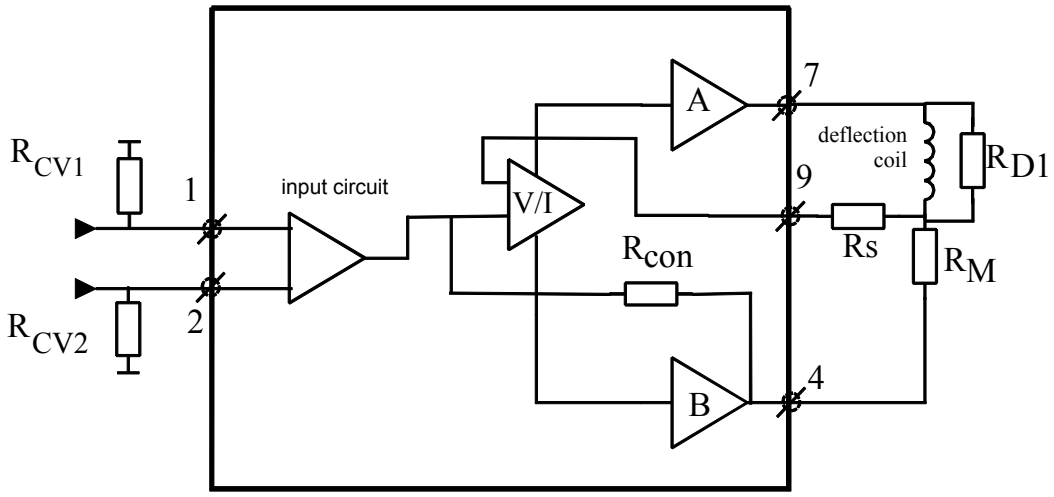



fig 4: Simplified block diagram of the vertical circuit.

Since the Input Stage (IS) is voltage driven, resistor $R_{cv1}$ and $R_{cv2}$ are used to convert the differential output current delivered by the driver circuit (See fig 4). But driver circuits, which deliver an output voltage can also be used, in that case resistor $R_{cv1}$ and $R_{cv2}$ are not necessary.

The voltage across the internal conversion resistor $R_{con}$ is compared with the output current through the deflection coil by means of a voltage current converter V/I which is measured as a voltage across $R_M$. The output amplifiers A and B will be driven until both voltages are equal. This means that the deflection current is determined by the ratio of the input resistors $R_{cv1,2}$ and the measuring resistor $R_M$.

The output current is adjustable up to 2.0 $A_{p-p}$ with the TDA8357J and up to 3.2 $A_{p-p}$ with the TDA8359J mainly by varying resistor $R_M$. The peak to peak input voltage should be as high as possible (maximum 1.5V) for having an optimal reducing of distortion on the input signals. The maximum input voltage (bias + peak voltage) is 1.6V. The minimum input voltage (bias - peak voltage) is 100 mV, however for an optimum linearity a minimum input voltage of 300 mV is recommended.

### 2.4 Vertical input circuit

**Pin 1 INA and pin 2 INB**

The input circuit is a differential voltage driven input. The input circuit is specially designed for direct connection to TV signal processors delivering a differential signal, but it is also suitable for single-ended applications See 2.4.2. For processors with output currents, the currents have to be converted to voltages by the conversion resistors $R_{CV1}$ and $R_{CV2}$ connected to pins 1 INA and 2 INB. Some type numbers of suitable drive circuits: TDA9151B, TDA9160A, TDA9162, TDA933X, TDA8366, TDA8367, TDA837X, TDA884X/5X (one chip family), TDA886X/7X/8X (bocma family), TDA935X/6X/8X and TDA955X/6X/8X (ultimate one chip family) and TDA485X (deflection processor family).

An example of the vertical drive output signal of an “ultimate one chip” family IC is given below. The drive signal depends on which drive circuit is used. In the ultimate one chip family, the zoom is standard enabled and is set to a value of 25 (dec) on a range of 0 – 63. This causes a small flat piece just before the start of the scan.

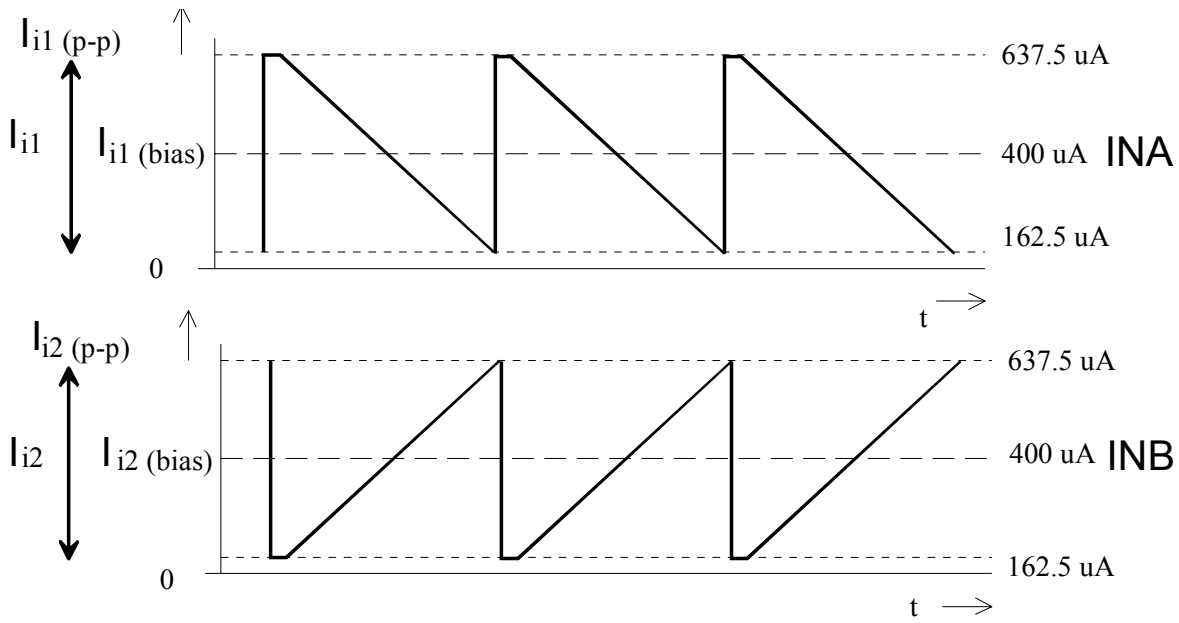



fig 5: Vertical drive output currents of the TDA935X/6X/8X / TDA955X/6X/8X family.

The bias output signal current is 400 μA typical. The differential mode peak to peak output current is typical 475 $\mu A_{P-P}$.

After connecting the TDA935X/6X/8X / TDA955X/6X/8X family to the TDA8357J / TDA8359J, the following waveforms appear on the input pin 1 INA and pin 2 INB when the conversion resistors $R_{CV1}$ and $R_{CV2}$ are 2k2. The voltage of INA shows a small uplift during the flyback time caused by the damping resistor compensation that consists of the compensation resistor $R_{CMP}$ and zenerdiode D4.

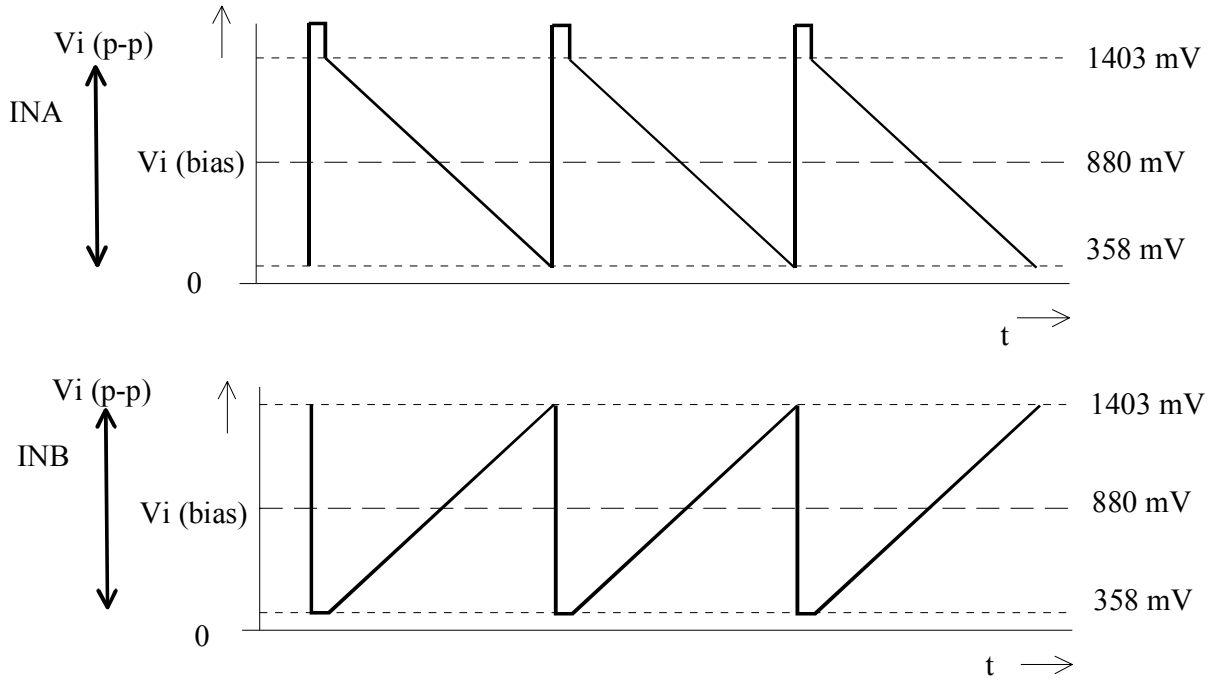



fig 6: Input voltages on pin 1 INA and pin 2 INB of TDA8357J / TDA8359J.

The differential voltage on the input ($V_{INA}$ - $V_{INB}$) is as follows:

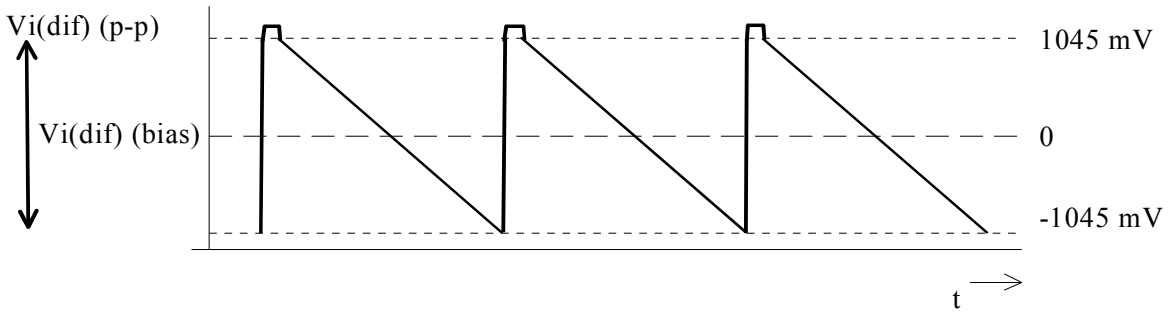



fig 7: Differential input voltage ($V_{INA}$ -$V_{INB}$)

The internal input configuration is symmetrical to have a good EMI behaviour, so the external input configuration should also be symmetrical. This means that the drive tracks should be as short as possible and routed next to each other.

The input configuration is as follows:

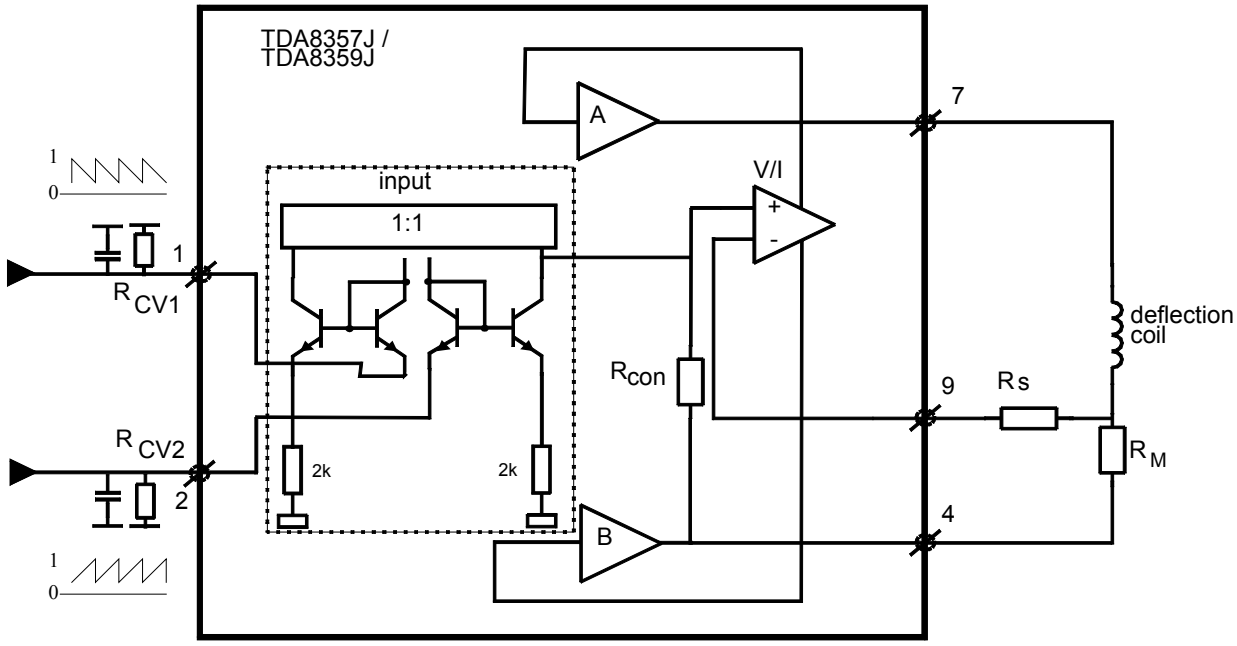



fig 8: Input configuration.

The differential input voltage is compared with the voltage across the measuring resistor $R_M$, providing the feedback information. The voltage across $R_M$ is proportional to the output current. The relationship between the differential input voltage and the output current is defined by:

$$V_{i(dif)(p-p)} = I_{o(p-p)} \times R_M$$

$$V_{i(dif)(p-p)} = V_{INA} - V_{INB}$$ (See fig 7.)

$V_{INA}$ = voltage INA
$V_{INB}$ = voltage INB
$I_{o(p-p)}$ = output current through the deflection coil and $R_M$, peak to peak value
$R_M$ = measuring resistor

The next figure gives the vertical drive circuit diagram of the TDA935X/6X/8X / TDA955X/6X/8X family with the vertical output stage TDA8357 / TDA8359J.

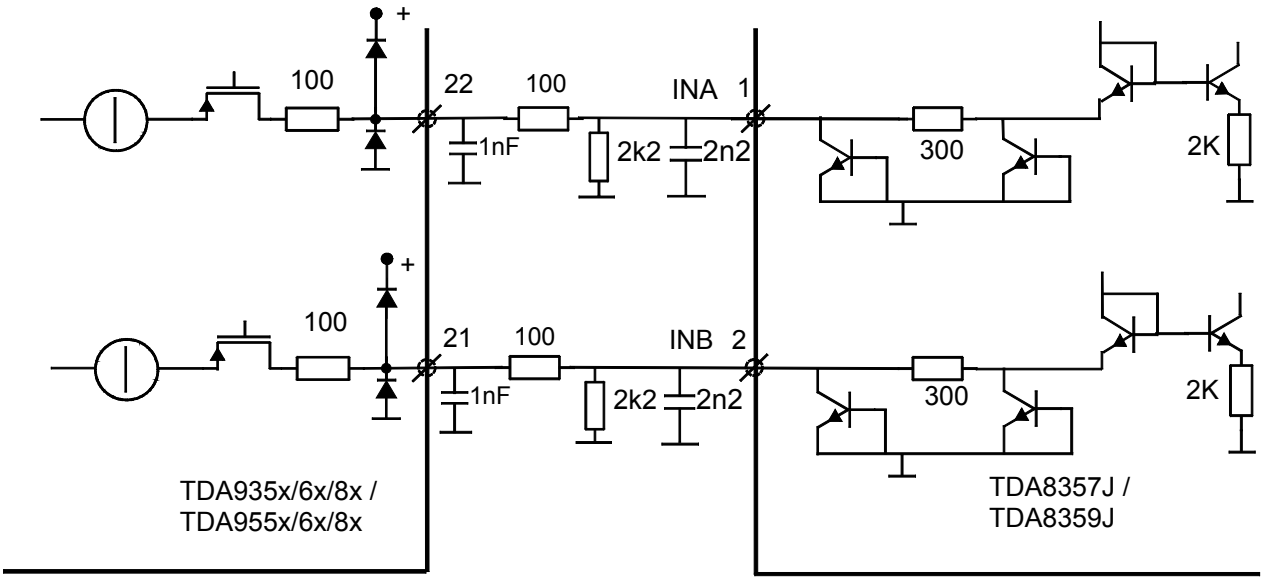



fig 9: Interconnect between TDA935x/6x/8x / TDA955x/6x/8x and TDA8357J / TDA8359J.

### 2.4.1 Conversion resistors $R_{CV1,2}$ and measuring resistor $R_M$

Most of the TV signal processors of Philips have a current output. This current has to be converted by resistors $R_{CV1}$ and $R_{CV2}$ at the input of the TDA8357J / TDA8359J.

The peak to peak input voltage $V_{I(p-p)}$ should be as high as possible (maximum 1.5V) for an optimal reducing of the differential distortion on the input signals. So $R_{CV1}$ and $R_{CV2}$ have to be chosen so that $V_{I(p-p)}$ is as high as possible. See fig 6. The maximum input voltage (bias + peak voltage) on pin 1 INA and pin 2 INB is 1.6V. The minimum input voltage (bias - peak voltage) is 100 mV, however a minimum input voltage of 300 mV is recommended because of an optimum linearity.

The conversion resistors $R_{CV1}$ and $R_{CV2}$ have the same value and can be calculated by: (See fig 5 and fig 6)

$$R_{CV1,2} = \frac{V_{i(bias)} + V_{i(peak)}}{I_{i1,2(bias)} + \frac{I_{i1,2(p-p)}}{2}} \quad \text{or} \quad R_{CV1,2} = \frac{V_{i(bias)} - V_{i(peak)}}{I_{i1,2(bias)} - \frac{I_{i1,2(p-p)}}{2}}$$

$V_{I(bias)} + V_{I(peak)}$ = should be <1.5V for room for vertical alignment. (max. input voltage =1.6V)
$V_{I(bias)} - V_{I(peak)}$ = should be > 0.3V for optimum linearity
$I_{I1,2(p-p)}$ = peak to peak output current given from the vertical deflection driver.
$I_{I1,2(bias)}$ = bias output current given from the vertical deflection driver

For the TDA935X/6X/8X or TDA955X/6X/8X family the value of $R_{CV}$ is:

$$R_{CV1,2} = \frac{V_{i(bias)} + V_{i(peak)}}{I_{i(bias)} + I_{i(peak)}} = \frac{1.5}{400 + \frac{475}{2}} = 2350\Omega$$

So $R_{CV1,2}$ must be 2k2

The output current is adjustable up to 2.0 $A_{p-p}$ for the TDA8357J and up to 3.2 $A_{p-p}$ for the TDA8359J by varying $R_M$.

The measuring resistor $R_M$ can be calculated by means of the formula:

$$R_M = \frac{V_{i(dif)(p-p)}}{I_{o(p-p)}}$$

$$V_{i(dif)(p-p)} = V_{INA} - V_{INB}$$

$$V_{i(dif)(p-p)} = I_{i1(p-p)} * R_{CV1} - (-I_{i2(p-p)} * R_{CV2})$$

Example for TDA8357J with the TDA935X/6X/8X or TDA955X/6X/8X family as driver:

We suppose the following:

$I_{O(p-p)}$ = 1.4 $A_{pp}$
$I_{i(p-p)}$ = 475µA (value is given by vertical driver)
$V_{i(p-p)}$ = 1045 mV (see fig 6)

$$V_{i(dif)(p-p)} = 475\mu A * 2k2 - (-475\mu A * 2k2) = 2.09V$$

$$R_M = \frac{2.09V}{1.4A} = 1.5\Omega$$

Example for TDA8359J with the TDA935X/6X/8X or TDA955X/6X/8X family as driver:

We suppose the following:

$I_{O(p-p)}$ = 2.4 $A_{pp}$
$I_{i(p-p)}$ = 475µA (value is given by vertical driver)
$V_{i(p-p)}$ = 1045 mV (see fig 6)

$$R_M = \frac{2.09V}{2.4A} = 0.87\Omega$$

### 2.4.2 Example of a single driven application with TDA8357J / TDA8359J

It is also possible to drive the TDA8357J / TDA8359J with a single drive signal, however differential driven is recommended. The single drive signal must be connected to pin 1 INA. Pin 2 INB needs then a stable DC voltage with a value of about the same as the bias voltage on pin 1 INA. A capacitor with a value of 10nF must be connected between pin 1 INA and pin 2 INB for stability. See fig 10. The measuring resistor $R_M$ must be half the value of when the TDA8357J / TDA8359J is differential driven. The compensation circuit ($R_{CMP}$ + $D_4$) equals as with differential drive, but the value of $R_{CMP}$ must be twice the value of when the TDA8357J / TDA8359J is differential driven.

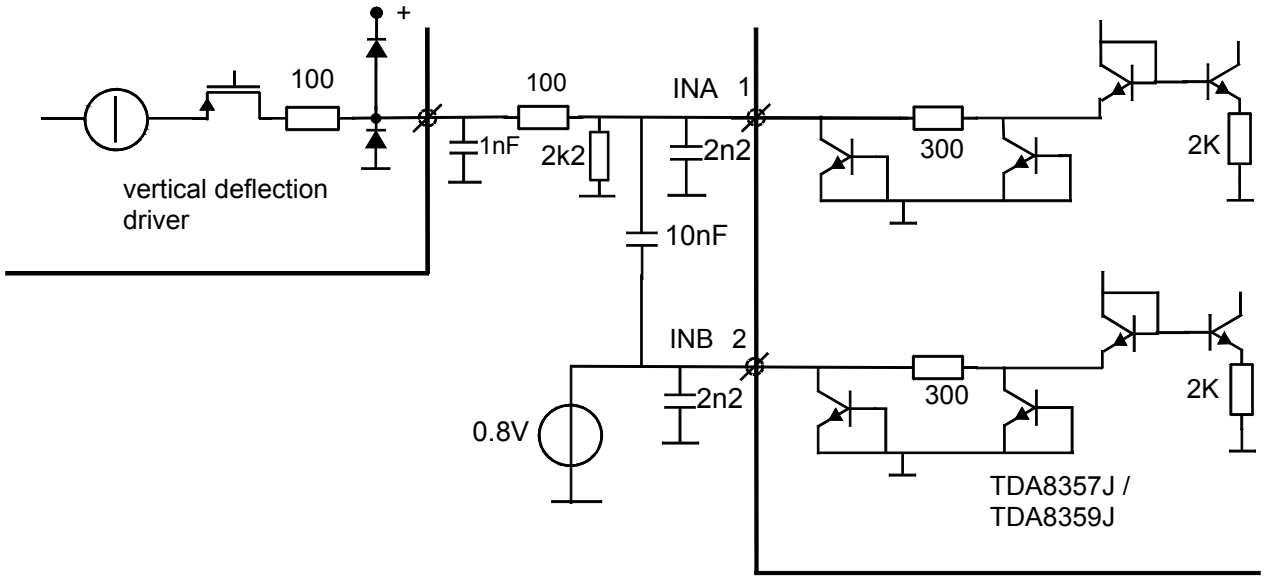



fig 10: Example of a single driven application

### 2.5 Feedback Circuit

**Pin 9 FEEDB**

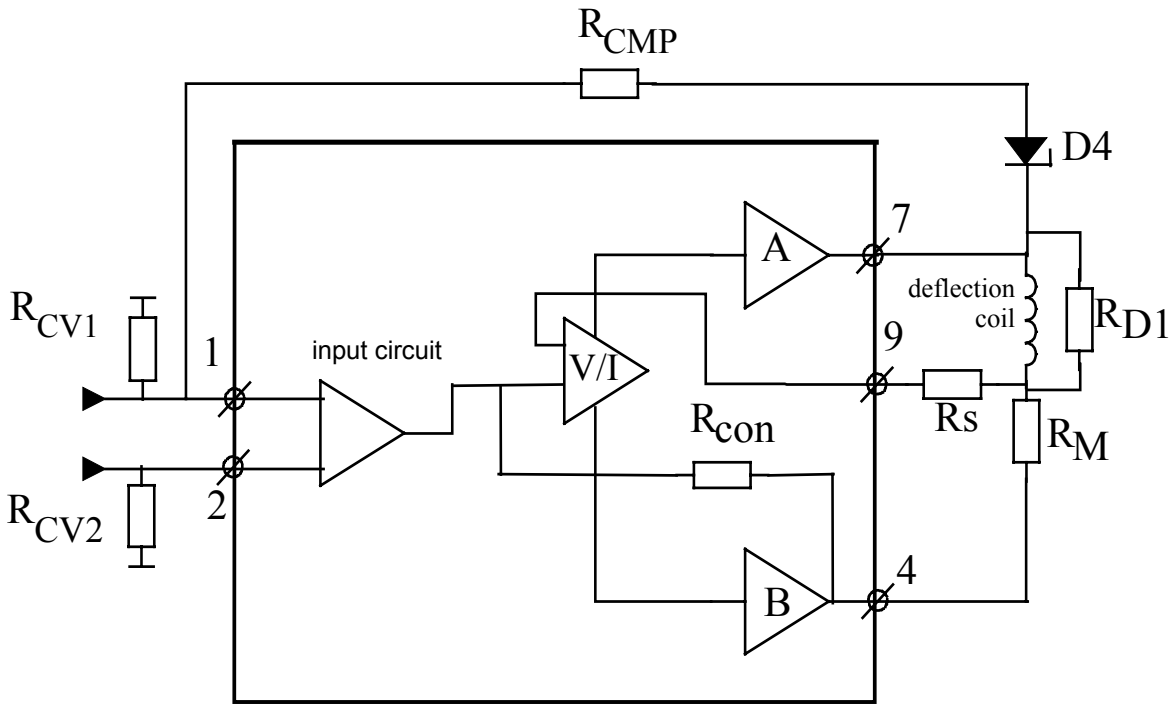



fig 11: Feedback circuit.

The feedback circuit is built up with a reference between pin 4 (OUTB) and pin 9 (FEEDB), the voltage across $R_M$ and a series resistor $R_S$ (pin 9). The input circuit is connected to a differential V/I converter, which compares the voltage across $R_M$ and the voltage across the internal conversion resistor $R_{CON}$. If both voltages are not equal the V/I converter drives the output stages until the voltage across $R_M$ is equal to the voltage across $R_{CON}$.

During flyback, the flyback voltage is put across the deflection coil and the damping resistor $R_{D1}$. This results in a higher current in the damping resistor and also in the measuring resistor. So the current in the measuring resistor is higher than the intended current in the coil. This affects the moment at which the flyback switch is not conducting anymore. To compensate this, an extra current is added to the current that flows through the conversion resistor $R_{CV1}$, by means of $R_{CMP}$ and $D_4$.

### 2.5.1 Series resistor ($R_S$)

The purpose of $R_S$ at pin 9 FEEDB is to achieve equal impedance for the V/I converter, $R_s = R_{con}$ because the V/I converter, see fig 11, should see equal input impedance at both inputs. This improves the common mode suppression. The tracks to the inputs are not the same. One track is connected internally to resistor $R_{CON}$. The other input has an external wire. To match $R_{con}$, the series resistor $R_S$ is connected between the deflection coil and pin 9. Choose the value of $R_S$ about 2.7kΩ.

If the output waveform should contain some oscillations, the value of $R_S$ can be slightly changed. A small capacitor of 1pF-100pF between pin 9 (FEEDB) and pin 4 (OUTB) could also help to suppress minor oscillations.

### 2.6 Vertical output stage

**Pin 4 OUTB, pin 7 OUTA and pin 9 FEEDB**

The Philips TDA8357J / TDA8359J vertical output stages use a class G bridge concept. (see fig 12).
In the class G concept the flyback supply voltage can be chosen independent from the main supply voltage. This allows a very efficient DC coupling of the vertical output stages. This matches perfectly with modern driving circuits, which can change settings like amplitude, shift, slope and s-correction, which are controlled via the $I^2C$ bus. The vertical deflection coil in series with resistor $R_M$ is connected between the two outputs pin 7 and pin 4. Resistor $R_M$ is used to measure the current through the coil. The voltage across resistor $R_M$ is the input voltage for the feedback stage.

The two output amplifier stages A and B are nearly identical. Output stage top MOSFET A (M2) and bottom MOSFET B (M3) and diode D1, conduct for the first part of the sawtooth (coil) current and are supplied from the main supply ($V_P$). Output stage top MOSFET B (M1) and bottom MOSFET A (M4) conduct for the second part of the sawtooth current and is supplied via the same main supply voltage.

MOSFET (M5) is the flyback switch. It is supplied through a higher supply voltage ($V_{FB}$) than the main supply voltage to achieve a short flyback time.
The maximum allowed values of the main supply voltage is 18 Volt and for the flyback supply voltage 66 Volt.

To prevent a short circuit between the main supply and the flyback supply, a diode (D1) is placed in series with the top MOSFET A (M2) of the output stage. To prevent conduction of the parasitic diode of the flyback switch (M5), (during the first part of the flyback period) a diode (D3) is placed in series with it.

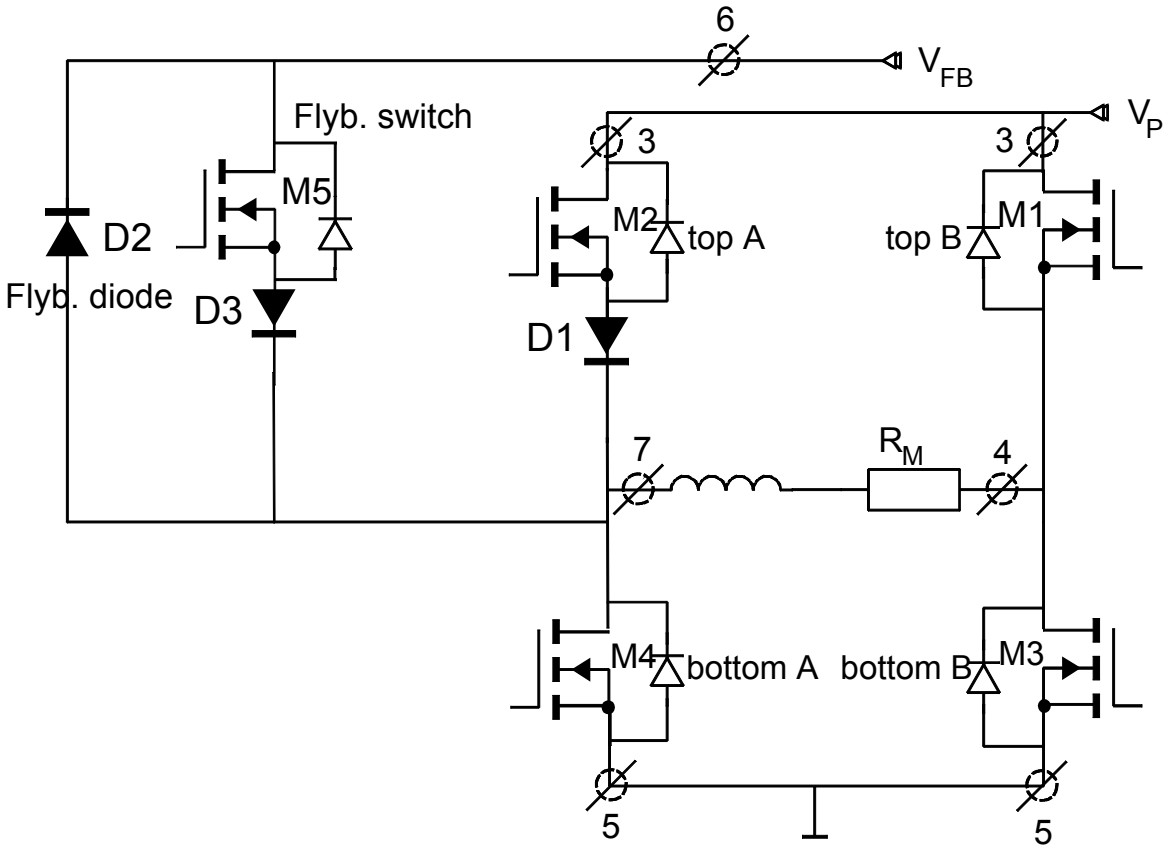



fig 12: Output configuration TDA8357J / TDA8359J.

The current flow through the output MOSFETs and the vertical deflection coil can be considered in four different parts/stages: the first part of the vertical scan, the second part of the vertical scan, the first part of the flyback and the second part of the flyback. The first and second part of the vertical scan will be discussed in this section, while the flyback part will be explained in the next section (2.7)

The current path in the vertical output bridge for the first part of the scan is illustrated by the dotted line in fig 13.
In this figure one can see that the current flows from the main supply pin via top MOSFET A (M2) and diode (D1) of output A in the vertical deflection coil and measuring resistor $R_M$, via bottom MOSFET B (M3) of output B to ground.

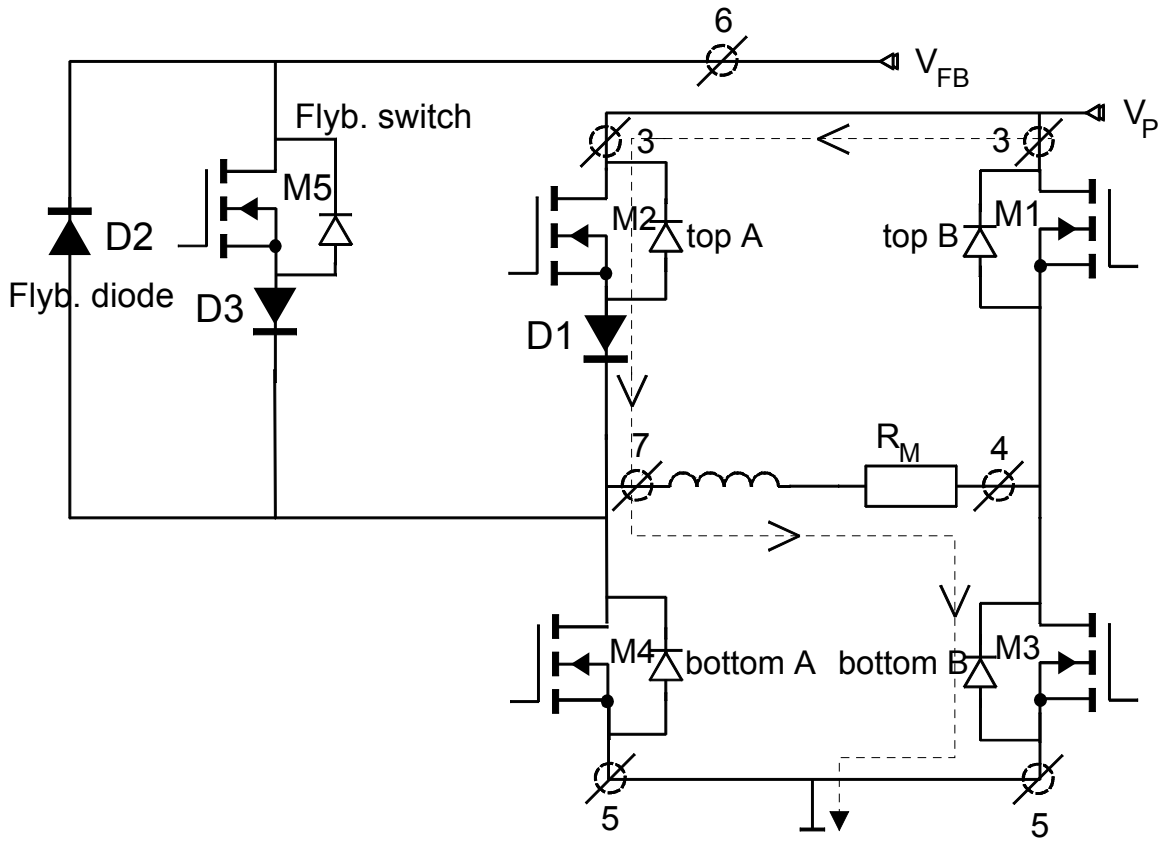



fig 13: Current path, first part of scan.

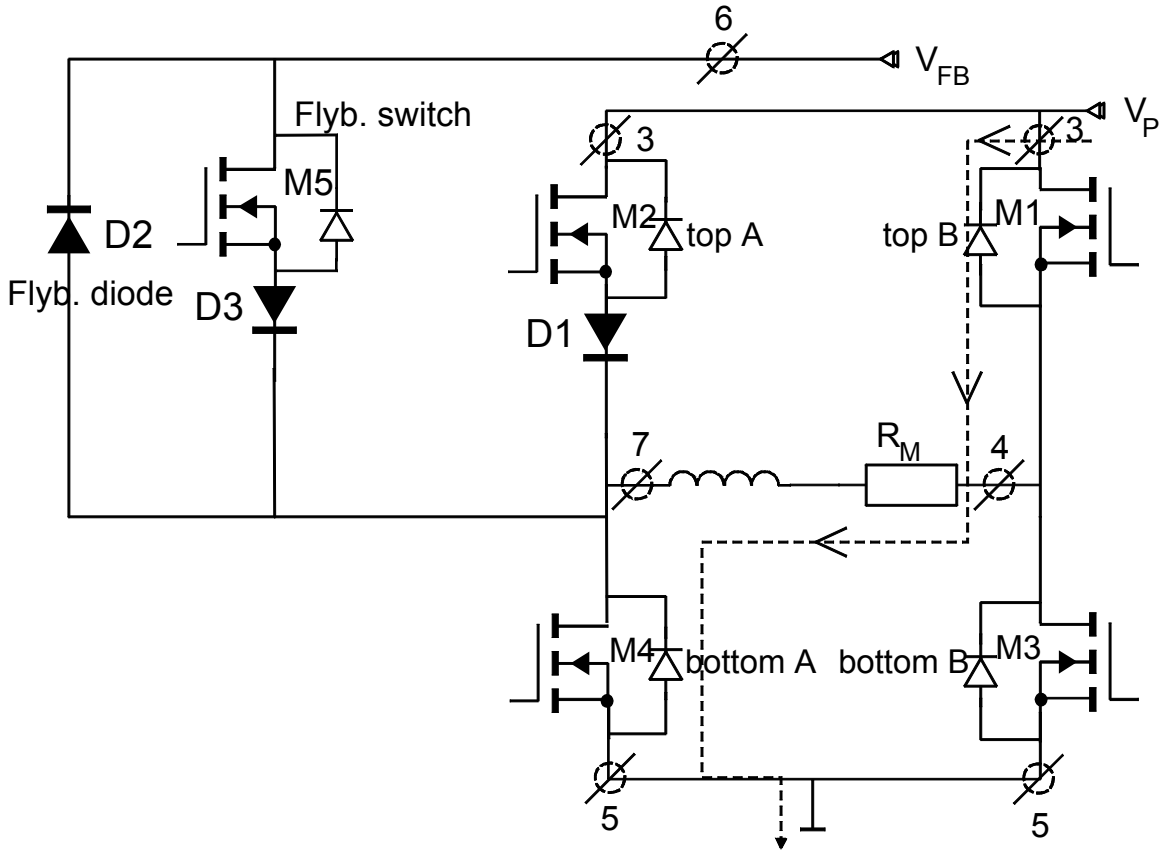



fig 14: Current path, second part of scan.

The current path for the second part of the scan is illustrated by the dotted line in fig 14. During the second part of the scan time, the current flows from the main supply pin via top MOSFET B (M1) via output B in the measuring resistor $R_M$ and the vertical deflection coil, via bottom MOSFET A (M4) of output A to ground. During the scan time, the current that flows through the deflection coil has a sawtooth shape and the main supply ($V_P$) supplies the current that is needed.

The supply current will be at it's maximum at the start of the scan, decreasing to the middle of the scan and than increasing until the end of the scan.

In fig 15 waveforms during scan are shown, these pictures are made with a digital oscilloscope. In this figure it is seen that the lines of output voltages A and B contain a small jump, when switching from the first part of the scan to the second part of the scan. This is because diode D1 causes a voltage drop. This is not crossover. The line of the output current is linear.

Furthermore one can see that the lines of the Output A voltage and the Output B voltage do not cross in the middle of the scan time. This is because the voltage drop across the deflection coil, for the first part of the scan is different than the voltage drop across the deflection coil during the second part of the scan. This is caused by the coil impedance, which exists of a resistive part and an inductive part. So the total voltage drop across the deflection coil exists of a resistive voltage and an inductive voltage. For the first part of the scan the inductive contribution and the resistive contribution are of opposite sign, while for the second part of the scan the inductive contribution and the resistive contribution have the same sign. See also section 2.11.1.

So, if the deflection coil has a *relatively large* L (inductance), the voltage drop during the *first part* of the scan has a *lower value* compared to the value of the second part of the scan.
That's why the crossing point of the lines of output A and output B shift to the left, when the L of the vertical deflection coil increases.

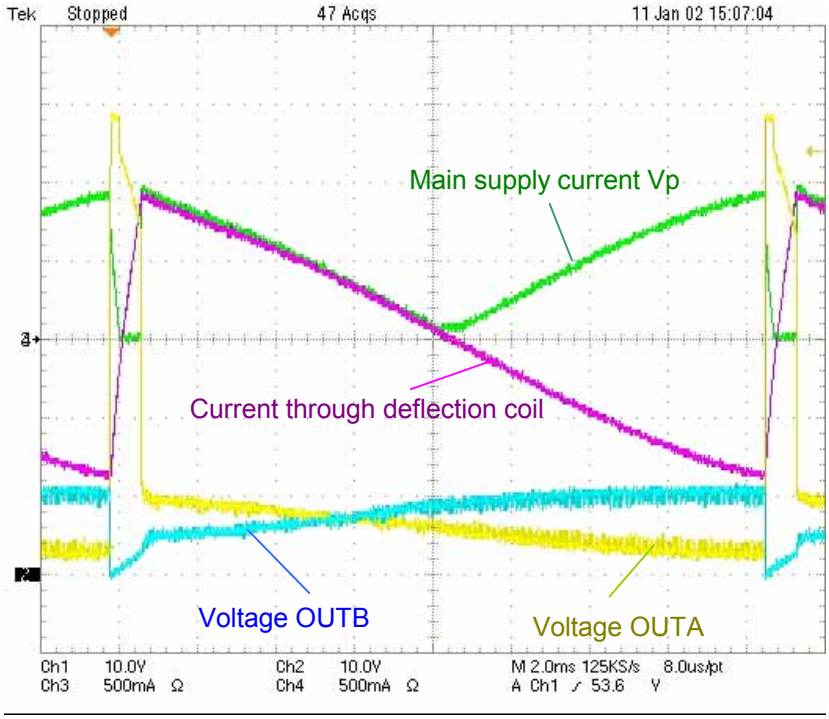



fig 15: Waveforms during scan.

### 2.7 The flyback switch

#### Pin 6 $V_{FB}$ and pin 7 OUTA

In the TDA8357J / TDA8359J concepts the value of the supply voltage ($V_P$) and the flyback supply voltage ($V_{FB}$) can be chosen independently (class G). In general, the flyback supply voltage will be chosen much higher than the supply voltage that is needed for the scan. A ratio of 2 to 4 is possible, with a maximum of 66 Volt. This is much higher than the value that is reached in conventional designs with a flyback voltage generator circuit (in general a ratio of 2, maximum). The flyback supply voltage is almost fully available at the output pin of stage A, thus across the deflection coil.

At the end of the scan time the input drive voltage will change fast in direction. The coil will try to maintain the present current level. At this moment the output signal cannot follow the input signal, which forces the amplifier into an open-loop condition. The flyback pulse will start.

The flyback can be divided in part A and B, see fig 16. Due to the high voltage across the coil and the influence of the damping resistor, the first part A has a short duration. Part A ends when the current in the deflection coil becomes zero.

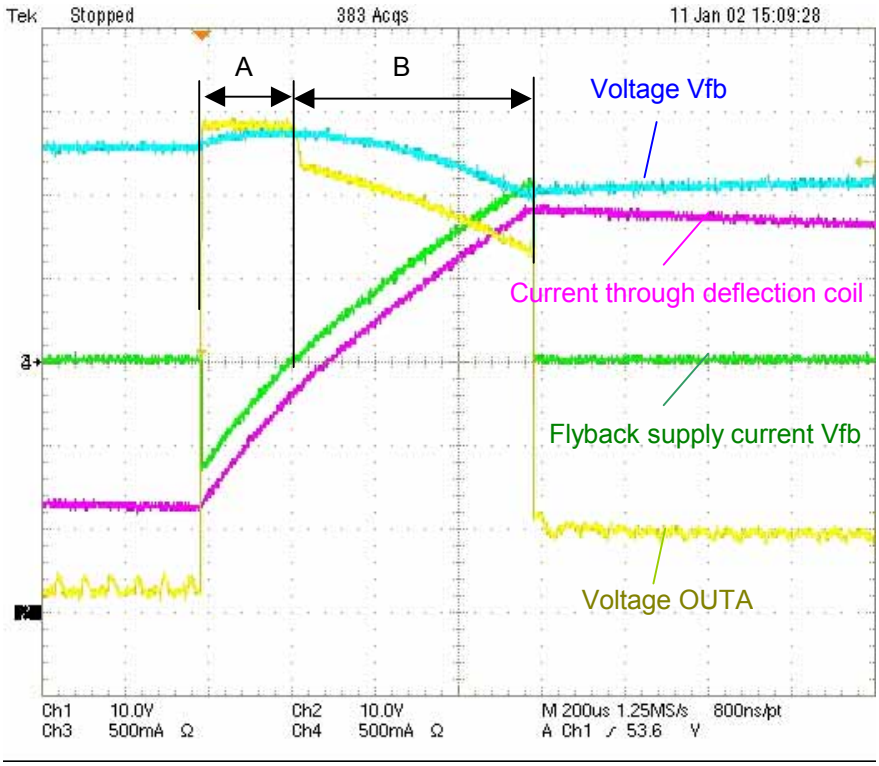



fig 16: Waveforms during flyback.

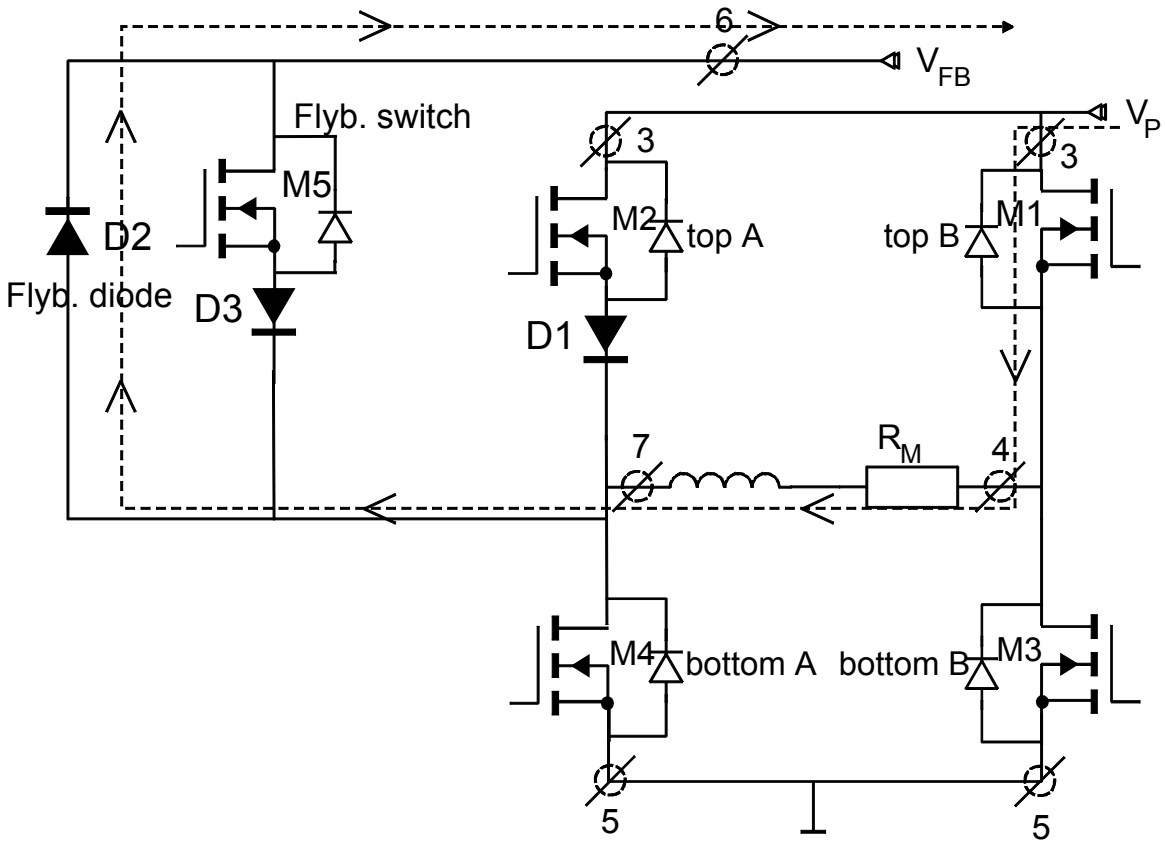



fig 17: Current path, first part of flyback.

At the start of the first part of the vertical flyback the internal drive signal switches off the top MOSFET of stage B (M1).
The current in the deflection coil seeks a way out and the voltage at the output pin 7 increases and so the voltage at pin 4 will drop and tries to go below zero. Now, a clamp circuit is activated to keep this voltage above zero. This clamp which will switch-on again MOSFET M1, otherwise the parasitic diode across bottom MOSFET M3 would conduct which could cause substrate-currents which could cause a malfunction of the device.
The voltage at the output (pin 7) increases and the flyback diode D2 conducts. This output voltage becomes about 2 Volt higher than the flyback supply voltage (=voltage across diode D2), see fig 16. The current is fed into the flyback supply capacitor.
The current goes now through the top MOSFET of stage B (M1), the external measuring resistor $R_M$, the deflection coil and the internal flyback diode (D2) into the flyback supply, see the dotted line in fig 17.

The current flow for the second part “B” of the vertical flyback is given below.

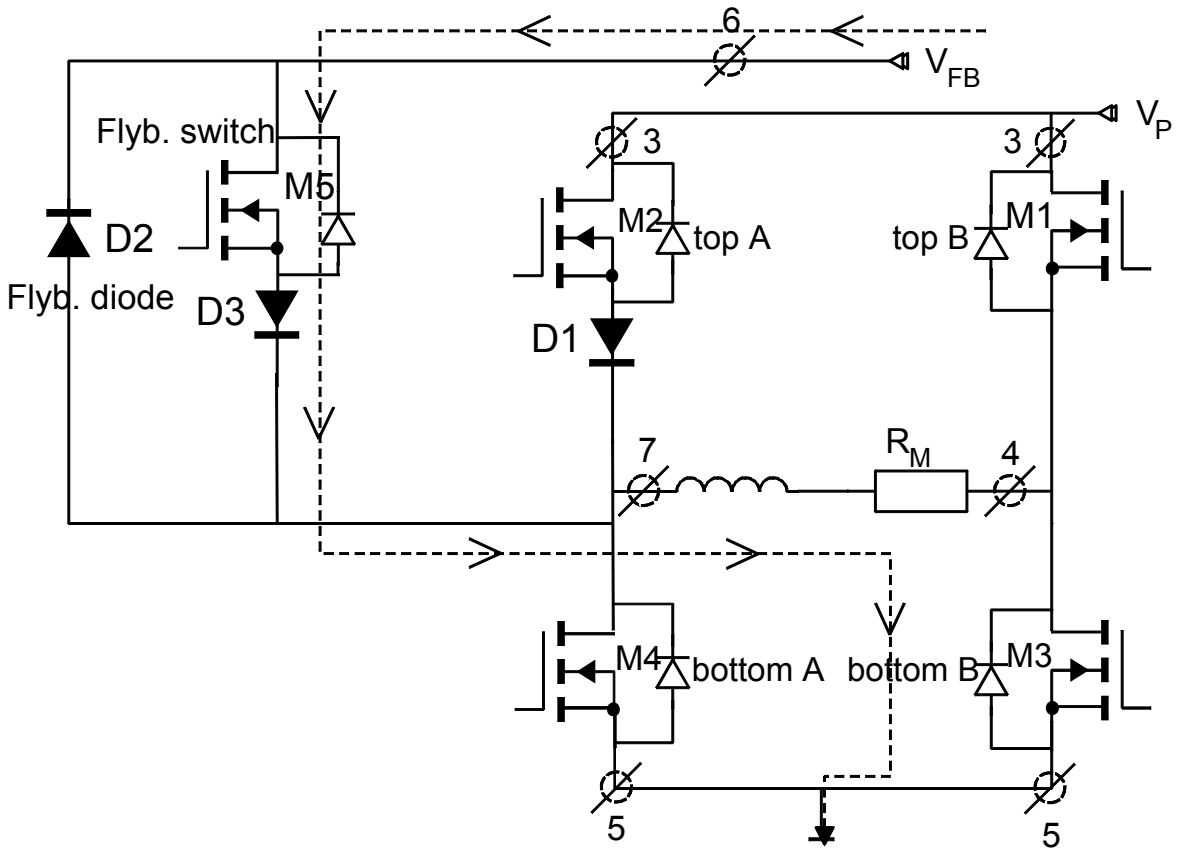



fig 18: Current path, second part of flyback.

The second part, part B of the flyback pulse, starts when the current in the deflection coil crosses the zero level, see fig 16. Now, the current in the deflection coil is supplied by the flyback voltage supply and the flyback switch (M5) conducts. The current flows via the flyback switch (M5), the internal diode (D3), the deflection coil, the measuring resistor $R_M$, via the bottom MOSFET of stage B (M3) to ground, see fig 18. (Due to a voltage loss across the flyback switch (M5) + the internal diode (D3), the output voltage at pin 7 is about 8 V lower than the flyback supply voltage. This voltage drop depends on the current in the coil; a higher current means a higher loss and thus a higher voltage drop.

The current through the coil will become positive now and will increase until the voltage value measured across $R_M$ equals the input voltage. Then the feedback loop is closed and the flyback switch is switched off. The scan sequence can start again.

### 2.7.1 Adaptive control of the flyback switch

The waveform during part B of the flyback waveform has a shape that is created by the adaptive control of the flyback switch, which operates as follows. The output current of the flyback switch is measured on a certain level onwards, the drive of the flyback switch is increased, thus lowering the impedance of the flyback switch at increasing flyback current, until it has reached a certain stable value. Now the end of the flyback has reached.

In the TDA8359JN2 / TDA8357JN2 the adaptive control circuit is activated at all values of the output current. This results in a lower dissipation in the flyback switch and a somewhat shorter flyback time. In the TDA8359JN1 / TDA8357JN1 the adaptive control circuit is not activated at a low output current. The small difference in the output voltage is given in fig 19:

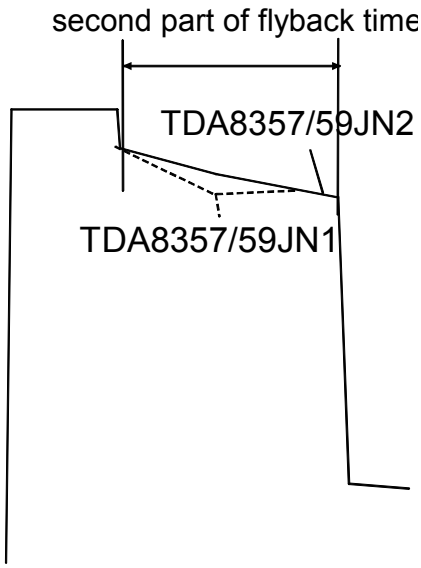



fig 19: Small difference in output voltage (flyback pulse) between N1 and N2

### 2.8 Damping resistor $R_{D1}$ and damping resistor compensation circuit

**Pin 1 INA and pin 7 OUTA**

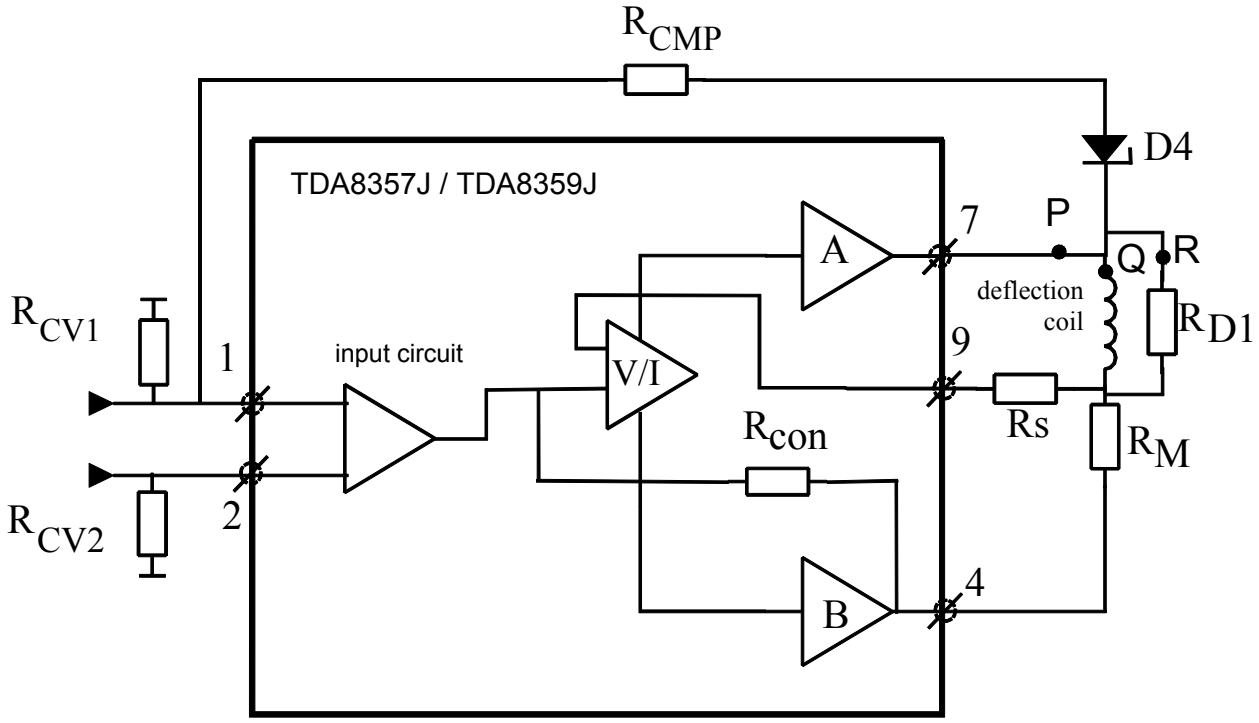



fig 20: Damping resistor compensation.

#### 2.8.1 Damping resistor $R_{D1}$

A damping resistor is connected across the deflection coil to smooth the switch points of the current and voltage as well to prevent ringing. The value of $R_{D1}$ depends on the deflection coil and it should be as high as possible. Choose the value of $R_{D1}$ about 270Ω. **Be aware that there can be a damping resistor mounted on the deflection coil on the picture tube.**

If the damping resistor is situated on the deflection coil on the picture tube, the following picture fig 21, is seen *by measuring the current through the wires from the PCB to the deflection coil connector* (point P in fig 20). The damping resistor causes the difference in current values between points P and Q during flyback. During the flyback time period a higher current flows through the damping resistor than during scan time due to a higher voltage across the deflection coil.

If the value of the damping resistor is too high, there will be too much horizontal distortion on the vertical output voltage. Then this distortion will be visible in the picture.

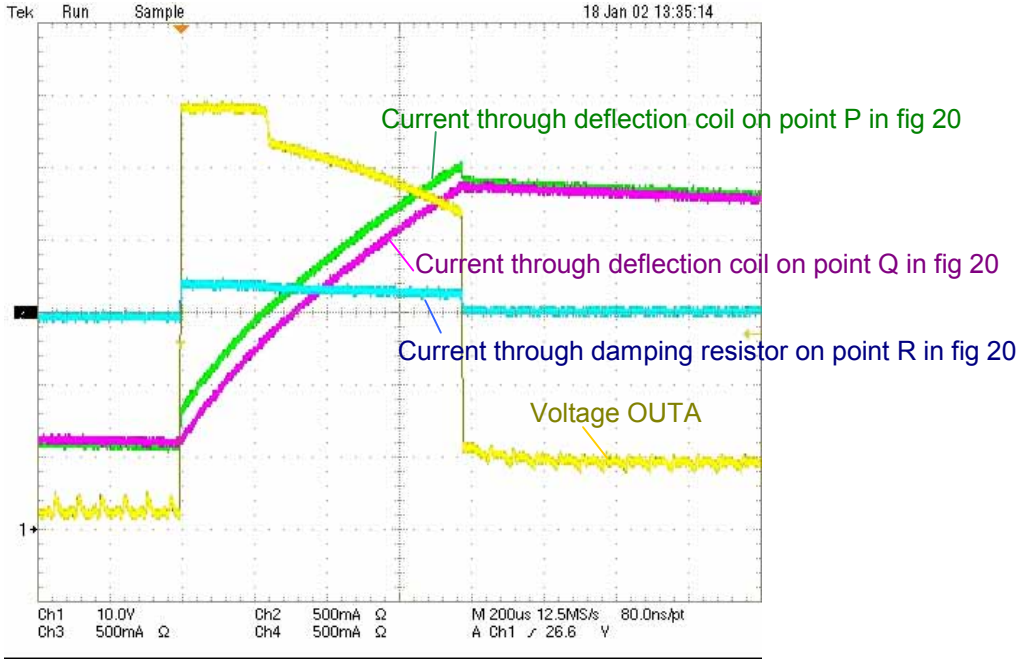



fig 21: Current through deflection coil measured on point P and Q in fig 20.

### 2.8.2 Damping resistor compensation circuit

The current values in the damping resistor $R_{D1}$ during scan and flyback are significantly different. During the flyback time period a higher current flows through the damping resistor due to a higher voltage across the deflection coil. Both the damping resistor current and the deflection coil current flow into the measuring resistor $R_M$. So a too low current flows into the deflection coil compared to the input signal during flyback time. This has an influence on the time the flyback switch is conducting. So without compensation the flyback switch stops conducting too soon and the flyback pulse width is too small. Now it will take a rather long time to reach the output current which equals the input signal. This results in a too low deflection coil current at the start of the scan.

The differences in the damping resistor current values during scan and flyback have to be externally compensated in order to achieve a short settling time. For that purpose a compensation resistor $R_{CMP}$ in series with a zenerdiode D4 is connected between pins OUTA and INA. The zenerdiode D4 should be equal to $V_P$ in order to compensate only during flyback time, when the voltage on OUTA is higher than $V_P$. See fig 20.

### 2.8.3 Calculation of the compensation resistor $R_{CMP}$

The value of the compensation resistor depends on:
- The flyback voltage supply; $V_{FB}$
- The internal voltage loss of the current path between pins $V_{FB}$ and OUTA. So the voltage loss across the flyback switch M5 and diode D3; $V_{loss(FB)}$. See fig 18.
- The voltage of the zenerdiode D4. Same as the supply voltage $V_p$.
- The value of the damping resistor; $R_{D1}$
- The value of the input resistors; $R_{CV1,2}$
- The peak to peak output current; $I_{o(p-p)}$
- The value of the deflection coil resistance in hot condition = $R_{coil(cold)} \times 1.2$
- The value of the measuring resistor; $R_M$

The compensation resistor $R_{CMP}$ is calculated in the following way:

$$R_{CMP} = \frac{\left(V_{FB} - V_{loss(FB)} - V_Z\right) \times R_{D1} \times R_{CV1}}{\left(V_{FB} - V_{loss(FB)} - \frac{I_{o(p-p)}}{2} \times R_{coil(hot)}\right) \times R_M}$$

Example of calculating $R_{CMP}$:

$V_{FB}$ = 30V
$V_{loss(FB)}$ = 8V
$V_Z$ = 14V
$R_{D1}$ = 270Ω
$I_{o(p-p)}$ = 2.4A
$R_{coil(hot)}$ = 6Ω x 1.2 = 7.2Ω
$R_M$ = 0.87Ω
$R_{CV1}$ = 2.2kΩ

$$R_{CMP} = \frac{(30 - 8 - 14) \times 270 \times 2200}{\left(30 - 8 - \frac{2.4}{2} \times 7.2\right) \times 0.87} = 409k\Omega$$

In the formula, only the voltage loss of the flyback switch is taken into account, but there is also a small voltage loss in output stage B. To correct the calculated value that is a little bit too high, round off the value downwards by means of choosing the next lower value in the E-range. So: $R_{CMP}$ = 390kΩ.

**So when a TV chassis used with different picture tubes with different $I_{o(p-p)}$ and $R_{coil}$, the value of $R_{CMP}$ has to be adapted with each picture tube.**

In fig 22, fig 23 and fig 24 are some oscilloscope pictures of an application, for different values of $R_{CMP}$. Pay attention to the differences in flyback time.

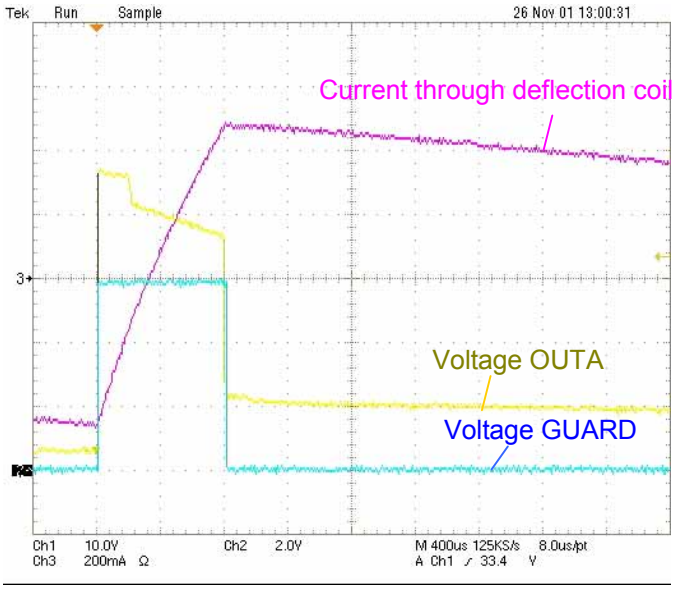



fig 22: Correct value of $R_{CMP}$.

In fig 22, the value of $R_{CMP}$ is correct. The result is a correct waveform of the coil current, output voltage and the vertical guard. The flyback time is 800 μs.

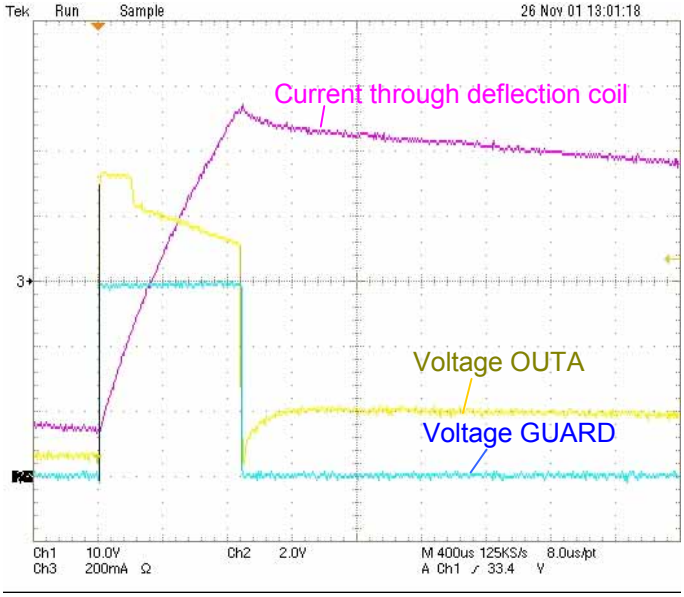



fig 23: $R_{CMP}$ too low, current overshoot at start scan / end flyback, too much compensation.

In fig 23 the value of $R_{CMP}$ is too low. The result is an overshoot condition in the output current and longer flyback time than in fig 21 (900 μs). Also the active high time of the vertical guard is longer than in fig 21.

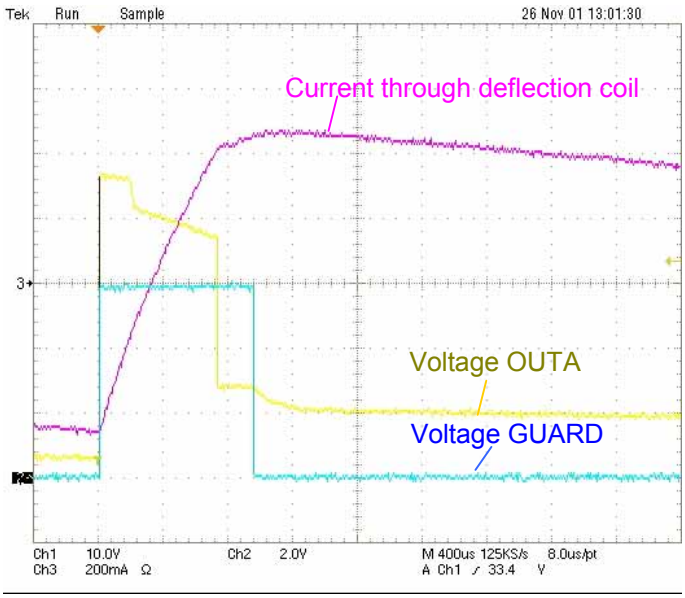



fig 24: $R_{CMP}$ too high, current undershoot at start scan / end flyback, too less compensation.

In fig 24 the value of $R_{CMP}$ is too high. The result is an undershoot condition in the output current and clipping of the output voltage to the supply voltage $V_P$. The output circuit has not yet reached the level as given by the input signal, this is similar to an open loop condition and the vertical guard remains high. So the active high time of the vertical guard is longer (1000 μs).

**Be aware that when $R_{CMP}$ does not have the correct value, the vertical guard signal of pin 8 GUARD has a different active HIGH time in comparison with the flyback time.**

### 2.9 Protection Circuits

The TDA8357J / TDA8359J circuits have protection circuits for:

- Too high crystal temperature.
- Over-voltage of output stage A.

#### 2.9.1 High crystal temperature

A temperature sensor is located on the die of the TDA8357J / TDA8359J. If this sensor detects a temperature of approximately 170 °C, the protection circuit activates. The protection circuit reduces the drive of the output stage and the current through the coil is reduced. The guard output becomes high and can be used to signal the vertical deflection driver that a fault condition occurred.

#### 2.9.2 Over-voltage output A

The over-voltage protection is activated, when the voltage of output stage A (pin 7 OUTA) increases above 70 Volt. During this condition, the protection circuit switches on MOSFET (M4) of output stage A, so M4 conducts and the output voltage at pin 7 OUTA decreases.

To prevent a short-circuit between pin 6 $V_{FB}$ and pin 7 OUTA, at active over-voltage protection, the flyback switch M5 is not conducting.

Output stage B is ‘self-protecting’ because if an over-voltage occurs at output stage B (pin 4 OUTB), the parasitic diode from the top MOSFET (M1), conducts and the current is led to the elco at pin 3 $V_P$. (This is not possible at output stage A, because diode D1 would block the current path to the elco at pin 3 $V_P$)

## 2.10 Vertical Guard Circuit

### Pin 8 Guard

The TDA8357J / TDA8359J have an internal vertical guard circuit, which delivers the guard signal to output pin 8 GUARD. This vertical guard circuit generates a pulse during every vertical flyback and at other conditions when the picture tube should be blanked. It can also be used to prevent the picture tube from burn-in, (due to faulty vertical deflection conditions) and as a vertical synchronisation signal to a microprocessor for e.g. On Screen Display. This guard pulse can be monitored by the vertical deflection driver.

The guard output is active (high) for one of the following conditions:

1. During the vertical flyback period.

2. During an open-loop condition of the TDA8357J / TDA8359J. The circuit of the TDA8357J / TDA8359J can see an open loop condition e.g. when the output voltage is clipping to the supply voltage $V_P$ or clipping to the ground level due to a too low value of $V_P$ or due to a too high value of the compensation resistor $R_{CMP}$.

3. During thermal protection of the TDA8357J / TDA8359J (See section 2.9.1)

The guard output stage is a current source. In most applications a load resistor on pin 8 GUARD is used. This load resistor is used for having a quicker fall time of the guard pulse.

**Be aware that when the compensation resistor $R_{CMP}$ does not have the correct value or the value of the main supply voltage $V_P$ is too low, the vertical guard signal has a different active HIGH time in comparison with the flyback time.**

### 2.10.1 Vertical guard with TDA935X/6X/8X/N2 / TDA955X/6X/8X family as vertical driver circuit.

#### 2.10.1.1 Pin BLKIN of driver

In the TDA935X/6X/8X and TDA955X/6X/8X family the vertical guard function can be combined with the black current measuring input, pin BLKIN. For a reliable operation of the protection system and to avoid that the black current stabilisation is disturbed, the end of the vertical guard pulse should not overlap the RGB measuring pulses. Therefor this guard pulse must end before the black current measurement line. **Taking a higher flyback supply voltage $V_{FB}$ is a way to make the guard pulse width smaller.** Or see section 2.10.1.3

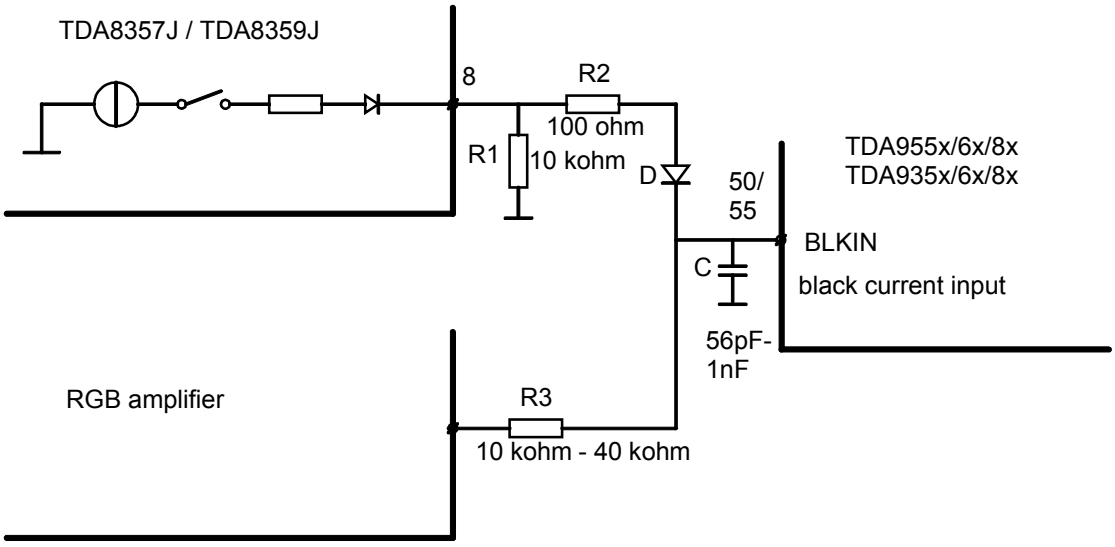



fig 25: Guard application for TDA955X/6X/8X / TDA935X/6X/8X family

In fig 25 is given the application for connecting the guard to the TDA955X/6X/8X / TDA935X/6X/8X family. Pin 8 GUARD of the TDA8357J / TDA8359J is connected to pin 50/55 BLKIN of the TDA955X/6X/8X / TDA935X/6X/8X family. The black-current measurement output of the RGB-amplifier is also connected to pin 50/55 BLKIN of the TDA955X/6X/8X / TDA935X/6X/8X family.

Load resistor R1 is used for optimising the fall time of the guard pulse. The value of R1 is 10kΩ.

When pin 8 GUARD is connected to BLKIN of the TDA955X/6X/8X / TDA935X/6X/8X family and the load resistor R1 is used, the black current measurement pulse is disturbed by R1. After the guard interval the TDA955X/6X/8X / TDA935X/6X/8X family starts the black level setting by measuring the leakage current. When this leakage current is measured, no extra load must be seen. So a diode D in series must be used for isolating the load resistor.

In fig 26 a scope picture of an application, which uses the guard function on pin BLKIN, is given. The TDA9587H is used as driver circuit.

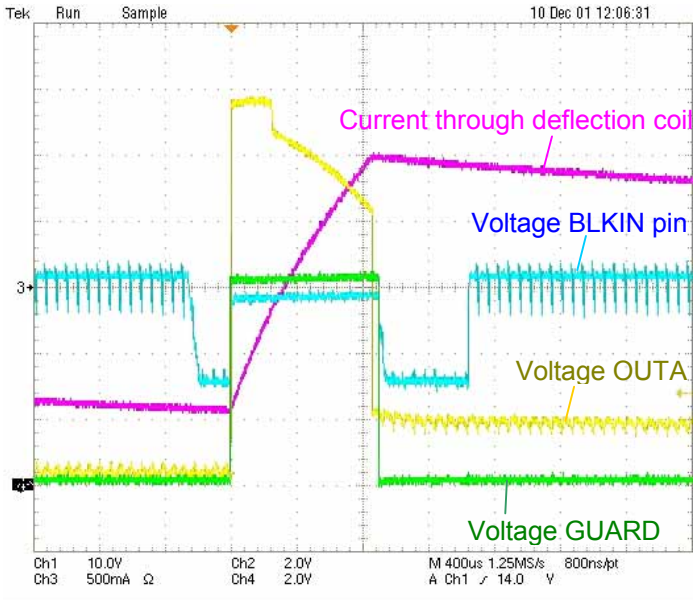



fig 26: Scope picture of application with vertical guard on BLKIN.

#### 2.10.1.2 Pin BCLIN of driver

In the TDA935X/6X/8X and TDA955X/6X/8X family the vertical guard function can also been combined with the beam current limiting input, pin BCLIN.

When pin 8 GUARD is connected to BCLIN of theTDA935X/6X/8X and TDA955X/6X/8X family and a load resistor of 10 - 12kohm is used, the beam current limiting circuit is disturbed. So a diode in series must be used for isolating the load resistor.

#### 2.10.1.3 Smaller vertical guard width

For a reliable operation of the protection system and to avoid that the black current stabilisation is disturbed, the end of the vertical guard pulse should not overlap the RGB measuring pulses. When the vertical guard pulse is too long, the circuit of fig 27 can be used to make the vertical guard pulse width smaller. See fig 28 for the result of the circuit of fig 27.

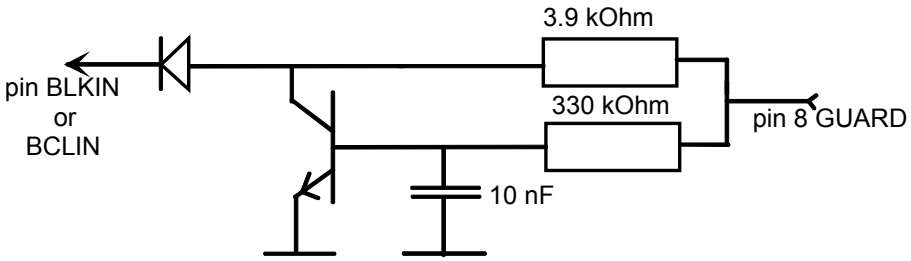



fig 27: Circuit for smaller vertical guard pulse width

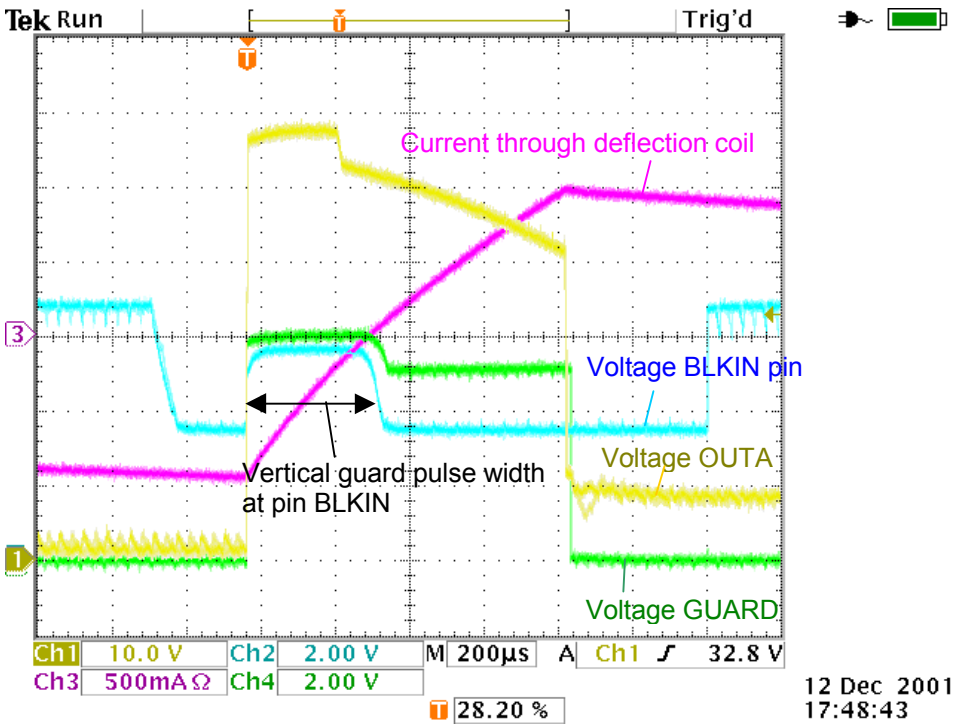



fig 28: Small vertical guard pulse width

### 2.10.2 Vertical guard with TDA884X/5X family as vertical driver circuit.

The TDA884X/885X family or other driver circuits can monitor the guard output, which generates a pulse. Whenever the height of this pulse is larger than 3.65 V the vertical deflection device works correctly. However for the TDA884X/885X family during scan the DC level may decrease below the 3.65 V level. Any other waveform is considered as failure and leads to blanking of the RGB outputs (see fig 29.)

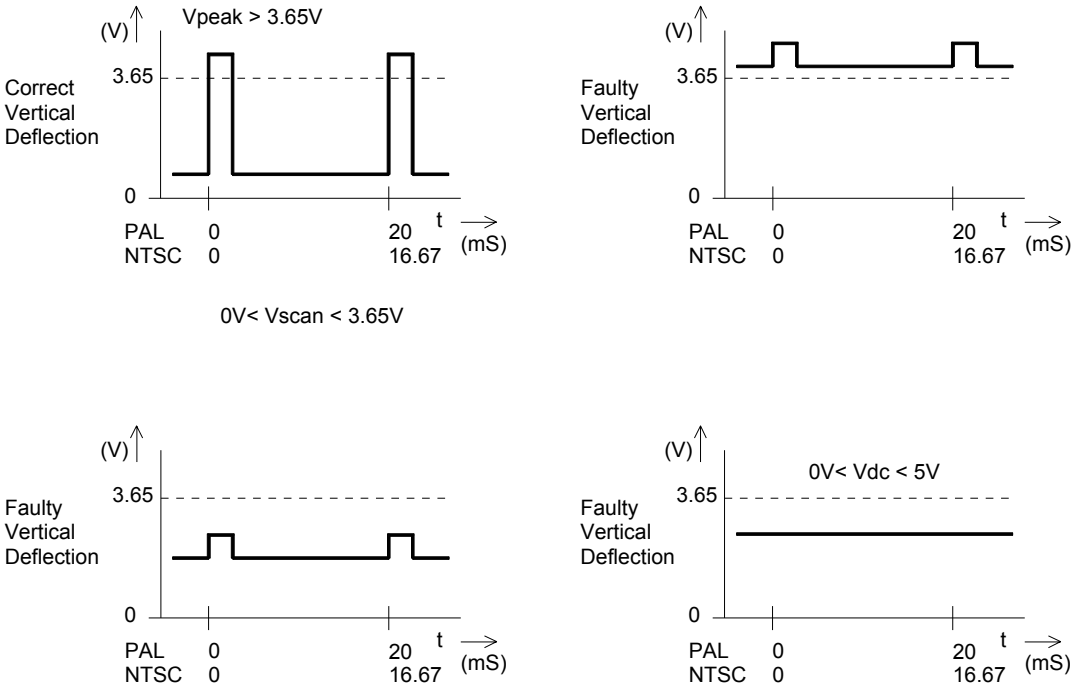



fig 29: Guard pulses with TDA884X/5X family

### 2.10.3 Vertical guard pulse connection.

In the next figure an application diagram is given which combines the two-beam current limiting functions (PWL and ABL) of a TDA884X/5X family device with the vertical guard function of the TDA8357J / TDA8359J.

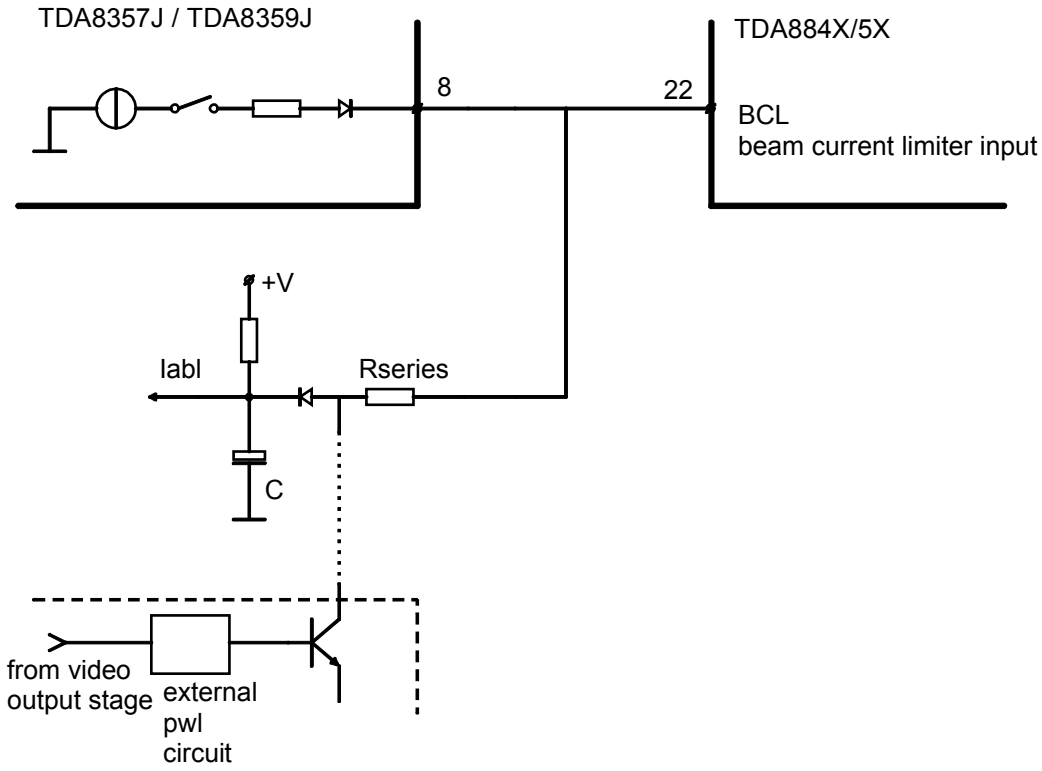



fig 30: Guard application PWL and ABL

The combined input of the TDA884X/885X family has the following characteristics:

* If the BCL is not active the voltage on pin 22 is 3.3 Volts, or higher.
* When BCL is active the internal impedance of pin 22 is 40 kOhm.
* The current that has to be pulled out the BCL-pin is constant.
  (Approximately 40µA) over the whole range.

The diode in series has two functions:

* preventing that the voltage at pin 22 can be driven above 3.65 Volts that can disturb the vertical guard function.
* Isolating pin 22 from capacitor C in order to ensure a fast PWL function of the TDA884X/5X family.

Important to know is that the BCL-circuit forms a load to the output signal of the vertical guard output circuit. This load should be below 1mA (at 4.5V pulse level). The min. series resistor at pin 22 can be calculated by:

$$R_{serie} = \frac{V_{guard} - V_{c\min} - V_{fdiode}}{I_{guard\max}} = \frac{3.65V - 0V - 0.65V}{1mA} = 3k\Omega \qquad V_{fdiode} \approx 0.65V$$

In this formula only the minimum voltage on the averaging capacitor is determined by the design of the ABL-function. (The minimum voltage on the averaging capacitor occurs at maximum beam current.)
In case $Vc_{min}$ = 0 V; $R_{series}$ = 3k. It is wise to use a higher value as series resistor therefore in fig 30, a value of 5.6k as $R_{series}$ has been chosen. Take also into consideration that in some applications $Vc_{min}$ can become negative.

### 2.10.4 Vertical guard pulse connection with high load (high current).

If the vertical guard pulse is also used as V-sync, take care that the maximum load is not exceeded. In this case it is possible to buffer first the vertical guard signal at the output of vertical deflection IC by means of a PNP-emitter follower. In order to separate the BCL-voltage on pin 22 from the buffered vertical guard (V-sync) signal, a diode from the emitter of the PNP to BCL-pin should be added, otherwise the vertical guard signal used as V-sync information will be disturbed (see fig 31).

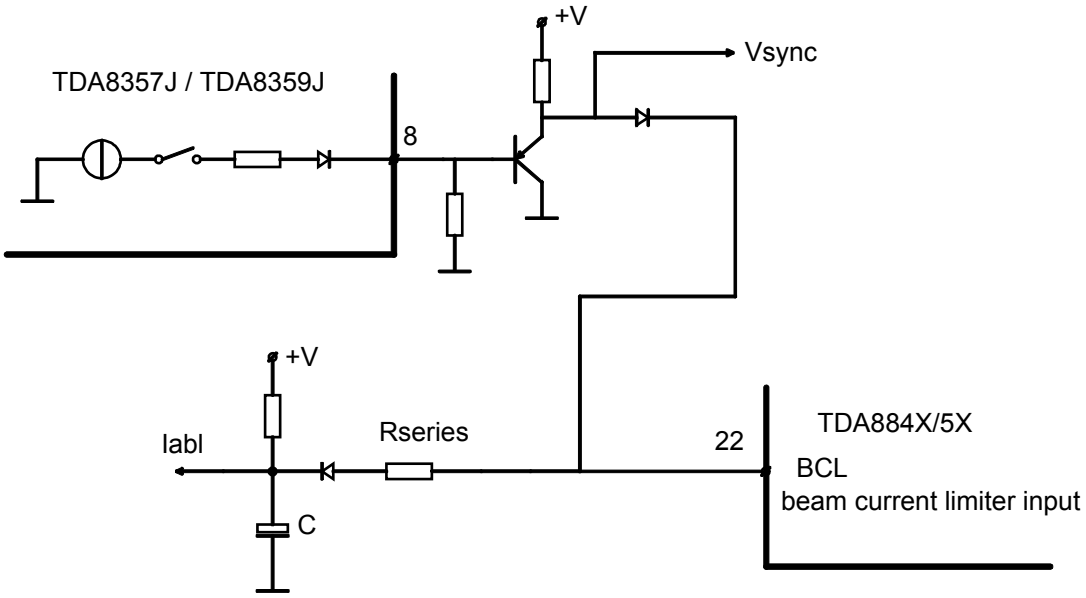



fig 31: Application for guard pulse with high load

### 2.11 Supplies

The TDA8357J / TDA8359J concepts have two power-supplies, a flyback supply and a main supply, which are calculated independently. The principle of operating with two supply voltages (class G) allows the use of an optimum main supply voltage $V_P$ for scan and an optimum flyback supply voltage $V_{FB}$ for flyback. This method achieves very high efficiency.

For having a stable supply current in the main supply $V_P$, a load capacitor with a value of 220 μF must be connected on pin 3 $V_P$. For having a stable supply current in the flyback supply current, a load capacitor connected on pin 6 $V_{FB}$ with a value of 47 μF will be sufficient.

#### 2.11.1 Calculation of the main supply $V_P$

**Pin 3 $V_P$**

There is a voltage drop across the coil during scan, which is determined by the coil impedance. The coil impedance exists of a resistive part and an inductive part so the total voltage drop across the coil exists of a resistive voltage and an inductive voltage. For the first part of the scan the inductive contribution and the resistive contribution are of opposite sign, while for the second part of the scan the inductive contribution and the resistive contribution have the same sign.

The internal output transistors have voltage losses. These voltage losses must be taken into account for calculation of the main supply voltage $V_P$.

The value of the internal voltage losses given by the output transistors can be found in the next graph (see fig 32). $V_{loss(1)}$ gives the voltage loss for the first part of the scan time. So $V_{loss(1)}$ is the sum of the voltage losses of MOSFET M2, diode D1 and MOSFET M3. $V_{loss(2)}$ gives the voltage loss for the second part of the scan time. . So $V_{loss(2)}$ is the sum of the voltage losses of MOSFET M1, MOSFET M4. See fig 12.

The difference of values between $V_{loss(1)}$ and $V_{loss(2)}$ is caused by the internal diode D1.

The difference of values of voltage losses between the TDA8357J / TDA8359J is caused by the difference in the size of the output transistors. In the TDA8359J the size of the output transistors are larger than in the TDA8357J. So the voltage losses are lower in the TDA8359J than in the TDA8357J.

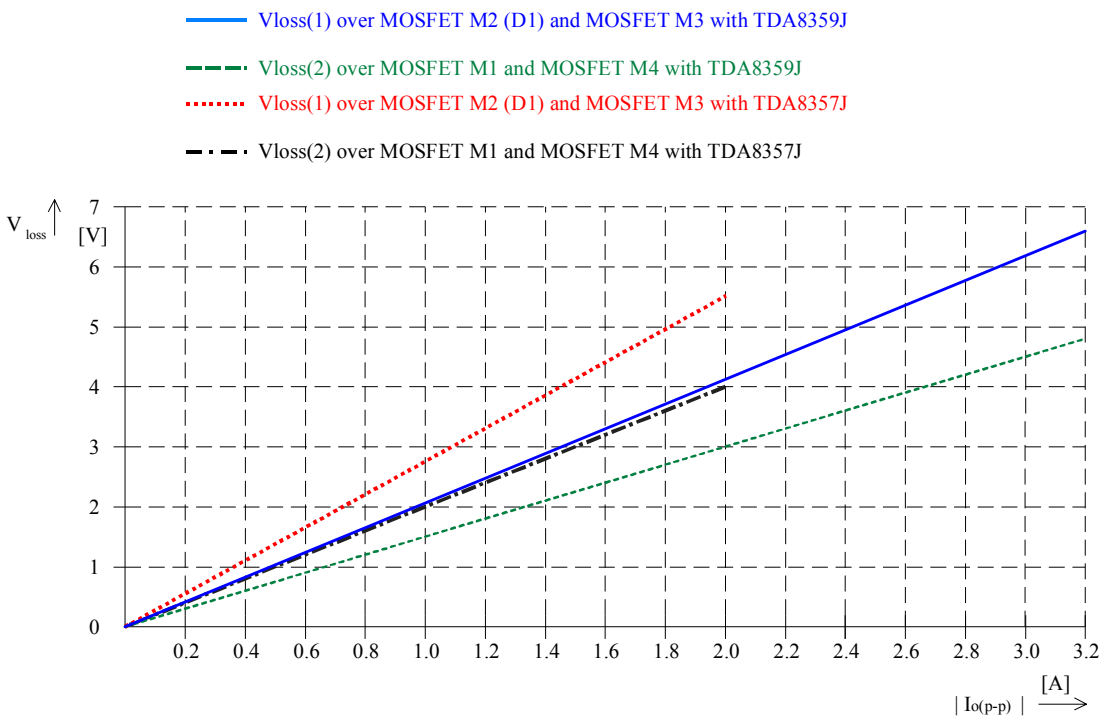



fig 32: Voltage loss of the output stage.

To calculate the minimum required supply voltage $V_P$, several specific application parameters have to be known:

- The peak to peak output current; $I_{o(p-p)}$
- The value of the deflection coil resistance in hot condition = $R_{coil(cold)} \times 1.2$
- The value of the measuring resistor; $R_M$
- The value of the deflection coil inductance; $L_{coil}$
- The value of the maximum vertical frequency; $f_{vert(max)}$
- $V_{loss(1,2)}$; see fig 32

The required power supply voltage $V_P$ for the first part of the scan:

$$V_{P(1)} = \frac{I_{o(p-p)}}{2} \times \left(R_{coil(hot)} + R_M\right) - L_{coil} \times I_{o(p-p)} \times f_{vert(\max)} + V_{loss(1)}$$

The required power supply voltage $V_P$ for the second part of the scan:

$$V_{P(2)} = \frac{I_{o(p-p)}}{2} \times \left(R_{coil(hot)} + R_M\right) + L_{coil} \times I_{o(p-p)} \times f_{vert(\max)} + V_{loss(2)}$$

Finally, after calculating the voltage supply by means of the above formulae, the minimum required value has to be the highest of the two values $V_{P(1)}$ and $V_{P(2)}$. This value has to be increased by 5% due to spread in the line output transformer and the deflection coil.

In the next example is shown how the main supply is calculated with TDA8359J:
We suppose the following:

$I_{o(p-p)}$ = 2.4 A
$R_{coil}$ = 6 Ω * 1.2 = 7.2 Ω
$R_M$ = 0.87Ω
$L_{coil}$ = 5 mH
$f_{vert(max)}$ = 50 Hz
$V_{loss(1)}$ = 4.9 V (see fig 32)
$V_{loss(2)}$ = 3.6 V (see fig 32)

**First part of scan:**

$$V_{P(1)} = \frac{2.4}{2} \times (7.2 + 0.87) - 5 \times 10^{-3} \times 2.4 \times 50 + 4.9 = 13.98V$$

**Second part of scan:**

$$V_{P(2)} = \frac{2.4}{2} \times (7.2 + 0.87) + 5 \times 10^{-3} \times 2.4 \times 50 + 3.6 = 13.88V$$

So we must choose 14 V and increase this value by 5% to get the minimum required supply voltage, $V_P$ = 14.7V.

**Be aware that when the value of $V_P$ is too low, the vertical guard signal of pin 8 has a different active HIGH time in comparison with the flyback time.** When the $V_P$ is too low, The output voltage of pin 7 OUTA is clipping to the $V_P$ at the beginning and end of the scan time. The circuit sees then an open loop condition and makes the vertical guard high.

### 2.11.2 Calculation of the flyback supply

**Pin 6 $V_{FB}$**

The flyback time is basically set by the value of the flyback voltage. So the flyback time can be optimised by choosing the appropriate flyback voltage. At the end of the flyback time, a settling time is needed at the start of the scan before the linear scan begins. Generally the settling time is covered by the overscan time. For the TDA8357J / TDA8359J the settling time is nearly zero if the compensation resistor $R_{CMP}$ has the correct value.

In a television application the value of the flyback time has to be shorter than the frame blanking time of the television standard. Mostly the flyback time starts half a line after the egalisation pulses. The flyback time must end before the generated measuring lines for the next frame. Generally in monitor applications a shorter time is needed, but that depends on the standard that is used.

In the next figure, the voltage across the coil during the flyback time is simplified as a voltage jump:

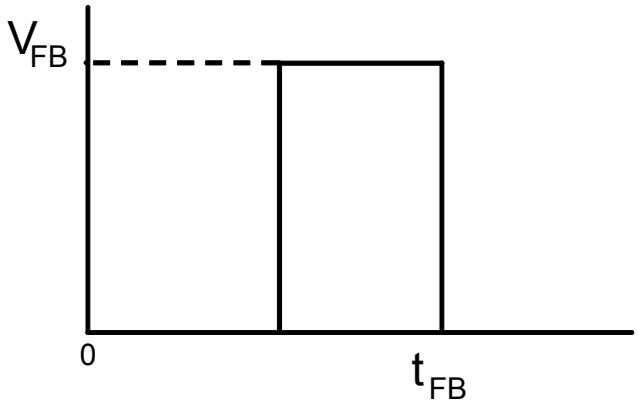



fig 33: Simplified flyback time.

To calculate the required supply voltage $V_{FB}$, several specific application parameters have to be known:

- The peak to peak output current; $I_{o(p-p)}$
- The maximum flyback current supply; $I_{FB(max)}$
- The flyback time; $t_{FB}$
- The value of the deflection coil resistance in hot condition = $R_{coil(cold)} \times 1.2$
- The value of the measuring resistor; $R_M$
- The value of the deflection coil inductance; $L_{coil}$

Using the simple model of fig 33, the flyback voltage $V_{FB}$ is calculated by:

$$I_{o(p-p)} = I_{FB(\max)} \times \left(1 - e^{-t_{FB}/x}\right)$$

Where: $I_{\max} = \dfrac{V_{FB}}{R_{coil(hot)} + R_M}$ and $x = \dfrac{L_{coil}}{R_{coil(hot)} + R_M}$

$$\Leftrightarrow I_{o(p-p)} = \frac{V_{FB}}{R_{coil(hot)} + R_M} \times \left(1 - e^{-t_{FB}/x}\right)$$

$$\Leftrightarrow I_{o(p-p)} \times \left(R_{coil(hot)} + R_M\right) = V_{FB} \times \left(1 - e^{-t_{FB}/x}\right)$$

so : $$V_{FB} = \frac{I_{o(p-p)} \times \left(R_{coil(hot)} + R_M\right)}{1 - e^{-t_{FB}/x}}$$

The simplified formula above assumes that the voltage during the flyback time is constant. Actually, in an application the flyback voltage is *not* constant during the flyback time. See also section 2.7.
The influence of the damping resistor ($R_{D1}$) can be neglected.

Furthermore there is no need to increase the flyback voltage to compensate the spread in the line output transformer and the deflection coil, because the calculated flyback voltage is about 5% to 10 % *higher* than required and is settled when the formulas above are used.

In the next example is shown how the flyback supply is calculated with TDA8359J:
We suppose the following:

$I_{o(p-p)}$ = 2.4 A
$R_{coil(hot)}$ = 6 Ω x 1.2 = 7.2 Ω
$R_M$ = 0.87 Ω
$t_{FB}$ = 640 μs
$L_{coil}$ = 5 mH

then :
$$x = \frac{0.005}{7.2 + 0.87} = 619.6 \times 10^{-6}$$

$$V_{FB} = 2.4 \times \frac{7.2 + 0.87}{1 - e^{-640 \times 10^{-6} \,/\, 619 \times 10^{-6}}} = 30.07V$$

So for the flyback supply voltage we choose 30 V.

### 2.12 SOAR behaviour output

TheTDA8357J / TDA8359J are designed in a 68-volt LVDMOS (Low Voltage DMOS) process. The advantage of using MOSFETs instead of bipolar transistors for the output stage is the absence of second breakdown. fig 34 shows the Safe Operating AREa of a bipolar transistor and of a MOSFET. It shows that the bipolar transistor delivers less current than the MOSFET, at a certain voltage. So a MOSFET output stage is more robust than a bipolar output stage. The restrictions for temperature are the same as those in the bipolar process.

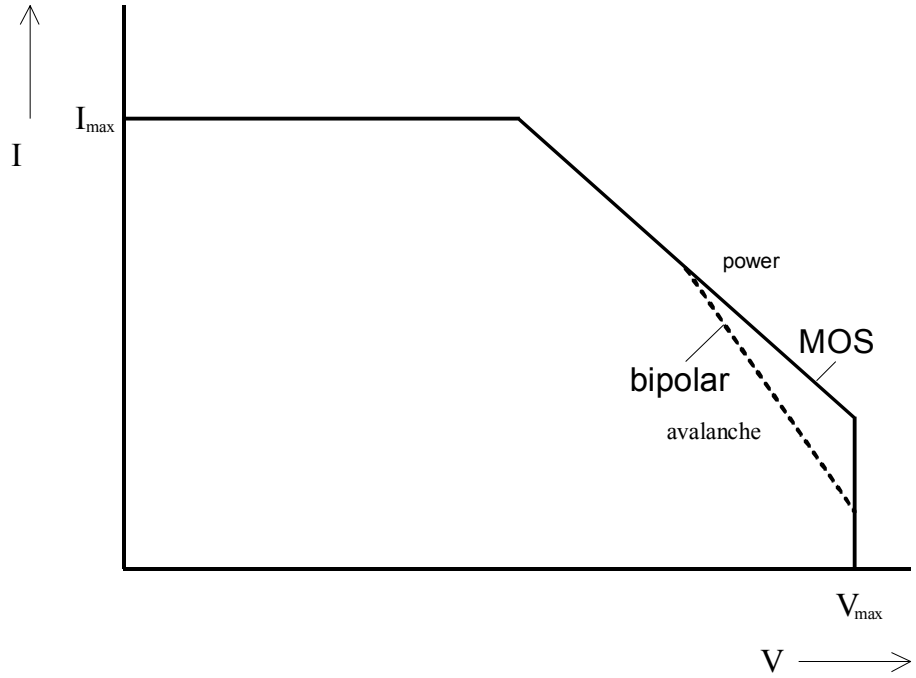



fig 34: Power limitations.

### 2.13 Power dissipation of the vertical output stage

The principle diagram of the bridge output stage is given in fig 35.

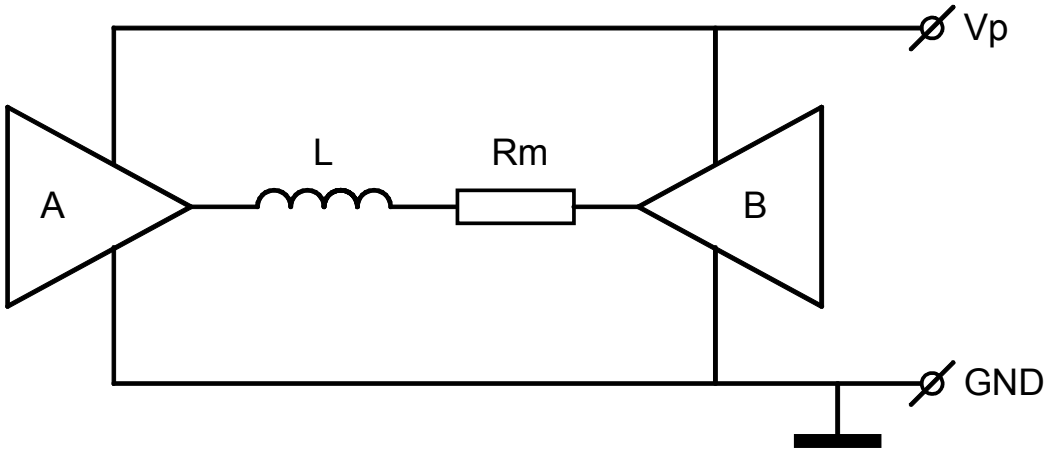



fig 35: Principle diagram.

The total power dissipation of the TDA8357J / TDA8359J is given by the formula:

$$P_{tot} = P_{sup} - P_L$$

where:

$P_{sup}$ = Power delivered by the supply
$P_L$ = Power dissipation of the load that consists of $R_{coil(hot)}+R_M$
$R_{coil(hot)}$ = The value of the deflection coil resistance in hot condition = $R_{coil(cold)} \times 1.2$
$R_M$ = The value of the measuring resistor

#### 2.13.1 Power $P_{sup}$

The power that is delivered by the supply is calculated by means of the next formula:

$$P_{sup} = \frac{V_P \times I_{sup}}{2}$$

or $$P_{sup} = \frac{V_P \times I_{o(p-p)}}{4}$$ because $$I_{sup} \approx \frac{I_{o(p-p)}}{2}$$

Where:

$I_{o(p-p)}$ = The peak to peak output current
$V_P$ = Voltage of the main supply

The explanation of the formula is described, step by step, in the Appendix (section 4).

The power that is delivered by the quiescent current of the TDA8357J / TDA8359J must also be taken into account:

$$V_P \times I_{q(P)(av)} = V_p \times 0.015$$

The contribution of the power during the flyback time is approximately 0.3W. This is an average value for the losses in the flyback supply.

So: $$P_{\sup} = \frac{V_P \times I_{o(p-p)}}{4} + V_P \times 0.015 + 0.3$$

### 2.13.2 Power dissipation $P_L$

The power that is dissipated by the load ($R_{coil}$ + $R_M$) is calculated by means of the next formula:

$$P_L = \frac{I_{o(p-p)}^2 \times (1.2 \times R_{coil} + R_M)}{12}$$

The explanation of the formula is described, step by step, in the Appendix (section 4).

### 2.13.3 Total power dissipation $P_{tot}$

Eventually the total power dissipation of the TDA8357J / TDA8359J is calculated by:

$$P_{tot} = P_{\sup} - P_L = \left[\frac{V_P \times I_{o(p-p)}}{4} + V_p \times 0.015 + 0.3\right] - \left[\frac{I_{o(p-p)}^2 \times (1.2 \times R_{coil} + R_M)}{12}\right]$$

Example of calculating $P_{tot}$ with TDA8359J:

Suppose:

$V_P$ = 14.7V
$I_{o(p-p)}$ = 2.4A
$R_{coil}$ = 6Ω (in cold condition)
$R_M$ = 0.87Ω

$$P_{tot} = \left[\frac{14.7 \times 2.4}{4} + 14.7 \times 0.015 + 0.3\right] - \left[\frac{2.4^2 \times (1.2 \times 6 + 0.87)}{12}\right] = 9.34 - 3.87 = 5.47W$$

### 2.14 Heatsink calculation TDA8357J / TDA8359J

The value of the heatsink can be calculated in a standard way with a method based on average temperatures. The heatsink must be chosen in such a way that the temperature of the die does not exceed the maximum allowable temperature of 150°C, as specified in the device specification.
**However, in general we recommend designing for an average die temperature that does not exceed 120°C.**

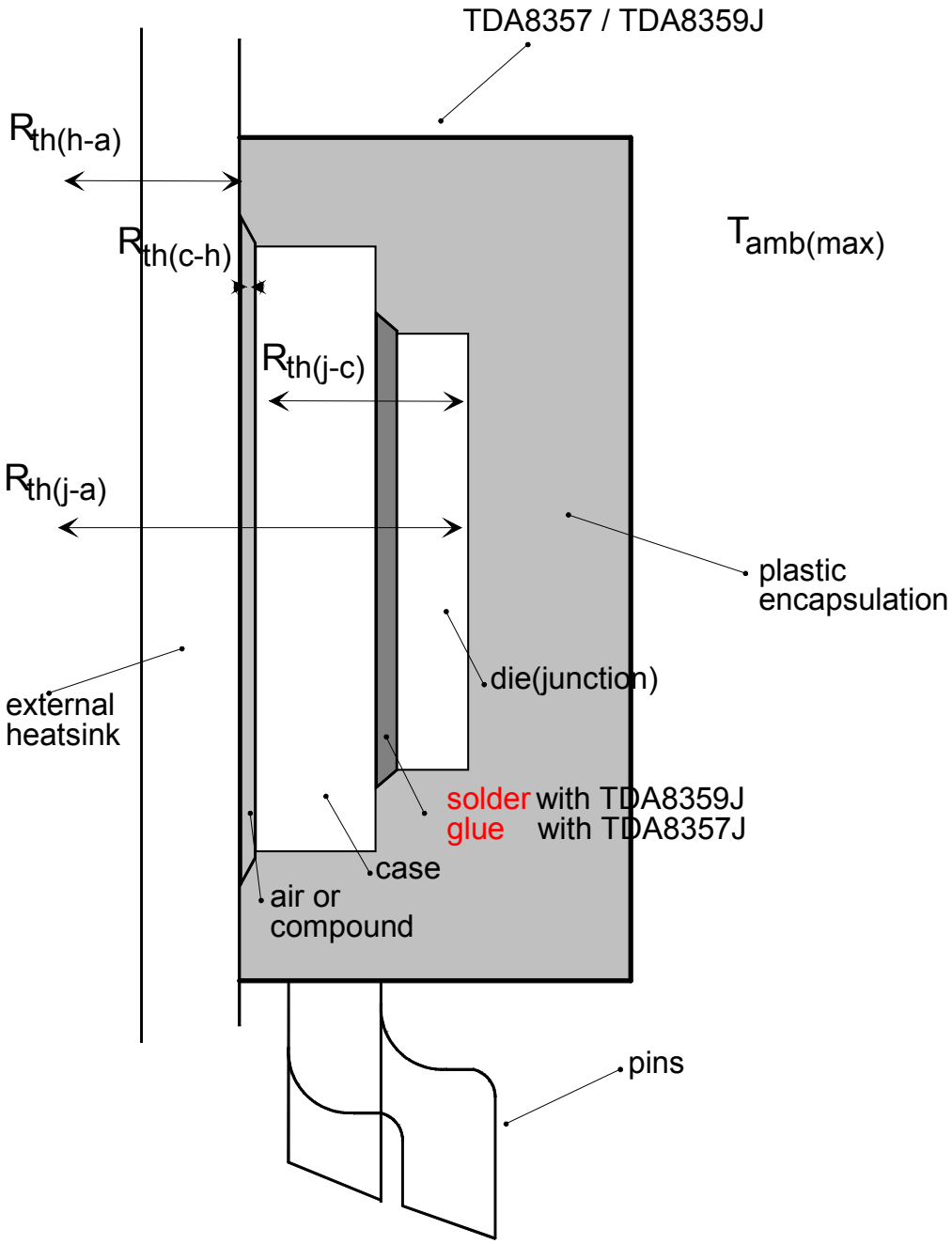



fig 36: Construction of the TDA8357J / TDA8359J mounted on a heatsink.

The construction of the TDA8357J / TDA8359J mounted on a heatsink is drawn in fig 36. In this picture several thermal resistances can be seen:

$R_{th(h-a)}$ = thermal resistance between heatsink and the ambient
$R_{th(c-h)}$ = thermal resistance between case and heatsink, depends on mounting method. See sec. 2.15
$R_{th(j-c)}$ = thermal resistance between die (junction) and case = 6 K/W for TDA8357J and = 3 K/W for TDA8359J
$R_{th(j-a)}$ = thermal resistance between die and ambient
$T_{amb(max)}$ = maximum ambient temperature
$P_{tot}$ = total power dissipation of the TDA8357J / TDA8359J
$T_j$ = temperature of the die

The thermal resistance $R_{th(j-a)}$ between the die and ambient is calculated by means of the next formulas:

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \quad \text{and} \quad T_j - T_{amb(\max)} = P_{tot} \times R_{th(j-a)}$$

$$\Leftrightarrow T_j - T_{amb(\max)} = P_{tot} \times \left(R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}\right)$$

$$\Leftrightarrow R_{th(h-a)} = \frac{T_j - T_{amb(\max)}}{P_{tot}} - \left(R_{th(j-c)} + R_{th(c-h)}\right)$$

The heatsink temperature $T_h$ can be calculated:

$$T_h = T_{amb(\max)} + \left(R_{th(h-a)} \times P_{tot}\right)$$

Example of calculating $R_{th(h-a)}$ with TDA8359J:

Suppose:

$T_j$ = 120 °C (We recommend this as maximum value)
$T_{amb(max)}$ = 40 °C
$P_{tot}$ = 5.5 Watt
$R_{th(j-c)}$ = 3 K/W
$R_{th(c-h)}$ = 2 K/W

$$R_{th(h-a)} = \frac{120-40}{5.5} - (3+2) = 9.55 K/W$$

The heatsink temperature will be:

$$T_h = 40 + (9.55 \times 5.5) = 92.53\,°C$$

It may be clear that, to *decrease* the temperature of the heatsink or the allowed temperature inside the cabinet, the dimensions of the heatsink should be *increased.*

### 2.15 Heatsink mounting

There is a direct electrical connection between the mounting base and the ground pin of the TDA8357J / TDA8359J. With TDA8357J the die is glued on the die pad and with the TDA8359J the die is soldered on the die pad and, see also fig 33. The heatsink can be connected to ground to achieve a better EMC behaviour.

The thermal resistance between case and heatsink $R_{th(c-h)}$ depends on the mounting method of the TDA8357J / TDA8359J on the heatsink. This can be clip or screw mounting. Both mounting methods can give acceptable results, if the instructions are followed. In general, screw mounting will result in lower $R_{th(c-h)}$ values than clip mounting. The main reason is the difference in press on force of the power encapsulation case to the heatsink.

Insulation between the case and heatsink can also be used, however this is in general not needed. When insulation is used, the $R_{th(c-h)}$ has a higher value.

A table is given below that shows the influence of the torque on the kappa value $R_{th(c-h)}$ with screw and clip mounting. The table clearly shows the difference in kappa value for dry mounting, mounting with heatsink compound and mounting with insulation.

| torque (Ncm) | heatsink compound (K/W) | | dry (K/W) | | with insulation (K/W) | |
|---|---|---|---|---|---|---|
| | screw | clip | screw | clip | screw | clip |
| 10 | - | 1.25 | - | 4.26 | - | 6.25 |
| 20 | 0.92 | 1.23 | 2.46 | 4.07 | 3.60 | 5.96 |
| 30 | 0.90 | 1.22 | 2.37 | 3.85 | 3.51 | 5.69 |
| 40 | 0.87 | 1.21 | 2.27 | 3.66 | 3.42 | 5.53 |
| 50 | 0.85 | 1.19 | 2.22 | 3.53 | 3.41 | 5.35 |
| 60 | 0.83 | 1.18 | 2.16 | 3.40 | 3.40 | 5.18 |
| 100 | - | 1.14 | - | 3.05 | - | 4.78 |

### 2.16 Flash-over.

Flashover is a random phenomenon at which the energy stored in the aquadag capacitor of the picture tube is discharged by a current that rushes through the electrodes of the CRT to find a way from inner to outer aquadag.

Loose conducting particles or whiskers on metal parts of the grids and cathodes cause flashes. Usually it finds first the focus grid. But a flash may also travel along the glass surface inside the neck, to exit at the socket of the picture tube. Thus, by means of one of these routes a flashover may reach every pin on the tube base. While the number of discharges varies from electrode to electrode, none of them are completely free from flashover. Extensive precautions are taken at manufacturing of the picture tube.

Furthermore, for soft-flash CRT, a high ohmic inner conductive coating reduces the peak flashover current to about a tenth of the value of that for hard-flash CRT. Nevertheless flashes may still occur. Sparkgaps and series resistors to the gun electrodes are required as primary safeguards. In the application of the vertical deflection amplifier one must pay attention to a proper PCB layout.

#### 2.16.1 Flash-over simulation

- The flash behaviour of a set can be simulated by means of a flash-mill.
- A flash mill consists of two brass ball electrodes, separated by a quartz disc.
- The disc provided with a hole rotates periodically by a motor between the pair of brass ball electrodes. When the hole is near the electrodes, a spark will jump between.

One wire of the flash-mill is connected to the EHT and the other is connected to the VG2 pin or the focus pin of the picture tube without series resistor.

#### 2.16.2 Flashover behaviour of TDA8357JN2 / TDA8359JN2

The TDA8357JN2 / TDA8359JN2 have improved robustness of the internal low substrate leakage current diodes against flashover by construction and a new process. Evaluation in several customer sets with only a small RC-filter (47nF + 1.5Ω) from pin 7 OUTA to pin 5 GND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during flash testing on critical pins like focus and VG2.

From our experiences with flashover and other overstress testing in the past it is recommended, see fig 37:

- HF decoupling capacitors of the supplies $V_P$ and $V_{FB}$ must be close to pins of the IC in the PCB-layout. These capacitors must be foil or MKT, not SMD.
- Grounding of all components to same ground as the IC: pin 5 GND. Avoid ground loops in the PCB-layout.

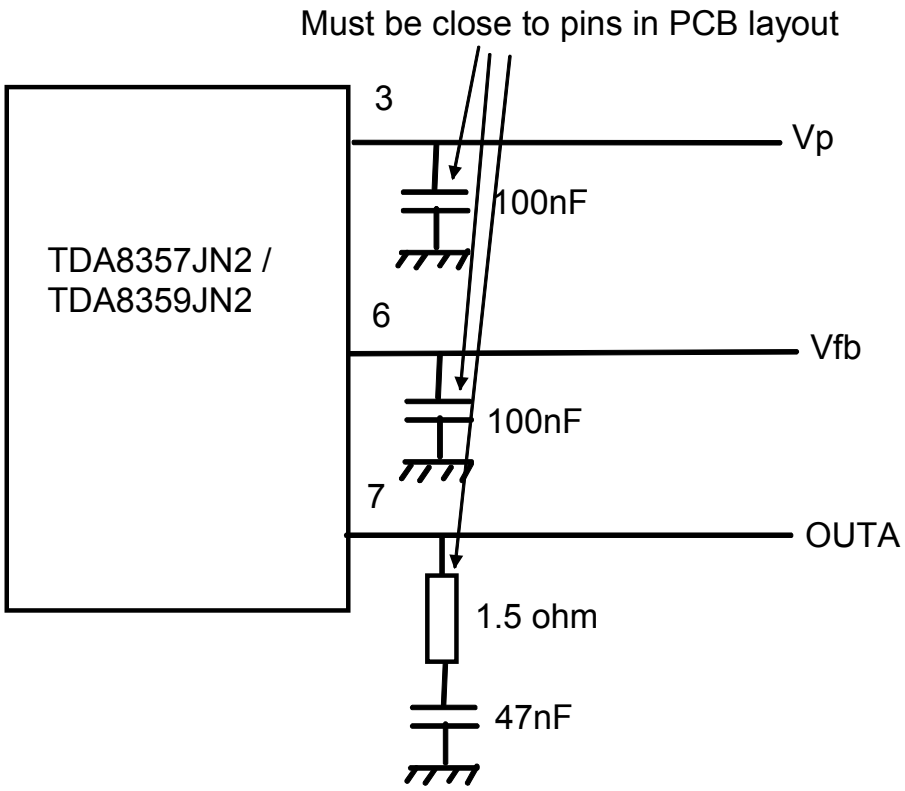



fig 37: Recommended layout for flashover protection

### 2.17 ESD-gun test

Next to the standard ESD-test on the TDA8357J / TDA8359J (Human Body Model and Machine Model), another ESD-test is introduced by some customers. This ESD-test is introduced to test the application, which the TDA8357J / TDA8359J is used in. This ESD-test is carried out by a standard ESD-gun (NSG 435), which is discharged on the connections of the vertical deflection coil mounted on the neck of the picture tube. The standard ESD-gun is discharged with a capacity of 150 pF and a series resistor of 330 Ω. This capacitor and resistor are standard IEC1000-4-2 (IEC 801-2, 1991) and are inside of the ESD-gun.

With the TDA8357JN1 / TDA8359JN1, some external components were needed for a better ESD-gun test behaviour. The TDA8357JN2 / TDA8359JN2 have improved robustness of internal low substrate leakage current diodes against overstress behaviour by construction and a new process. Evaluation in several customer sets with only a small RC-filter (47nF + 1.5Ω) from pin 7 OUTA to pin 5 GND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during ESD-gun testing up till 16.5 kV air discharge.

From our experiences with ESD-gun testing in the past it is recommended:

- HF decoupling capacitors of the supplies $V_P$ and $V_{FB}$ must be close to pins of the IC in the PCB-layout. When the HF decoupling capacitor of the flyback supply $V_{FB}$ is not close to the pin $V_{FB}$, the robustness is much lower. These capacitors must be foil or MKT, not SMD.

- Grounding of all components to same ground as the IC: pin 5 GND. Avoid ground loops in the PCB-layout.

### 2.18 EMC behaviour

When problems are found around the EMC behaviour of the application, the problems should be split into:

1. Susceptibility problem (radiation coming from outside of the IC).
2. Radiation problem (coming from the IC itself).

In both cases it is important to know the frequency that causes the problem(s).

Recommendations:

Reduction of the susceptibility and radiation can be achieved by:

- limit the bandwidth of the system.
- keep loop areas small to reduce magnetic pick up.
- keep sensitive tracks short to reduce electrical pick up.

A. **Bandwidth of the noise**
The bandwidth can be limited by filtering the input, output and power supply. Pay attention to small loop areas and short tracks during the design of the layout of the printed circuit board.

B. **Drive signal**
The drive signal tracks from the drive circuit to the TDA8357J / TDA8359J should be routed close to each other and made as short as possible. This is to minimise the loop area.
To suppress (EMC) interference it is possible to insert a series resistor of 100Ω – 1kΩ in the drive signals close to the driver. Furthermore capacitors can be used on the pins of the driver with a value of 560pF – 1Nf. In general, the use of small decoupling capacitors of 2.2 nF between the input pins and ground will solve problems at the input side. The capacitors must be connected directly to ground (pin 5) of the TDA8357J / TDA8359J. This has to be done with short wires and tracks in order to minimise parasitic inductance.

C. **Power supplies**
It is recommended to decouple the power supplies locally and as close as possible to the TDA8357J / TDA8359J. Especially the high frequency decoupling capacitor must be connected as close as possible to the pins of the IC. The main power supply and the flyback power supply, should be both decoupled with 100nF capacitors.

D. **Deflection coil**
The connection to the deflection coil is usual done with relatively long wires. These ‘long’ wires behave as an aerial, which picks up RF disturbances. If two blocking inductors of 2 µH are placed in these wires, a good blocking of the disturbance is achieved. The inductors can be implemented as a "bead on wire".

E. **Heatsink**
For good EMC behaviour the heatsink should be grounded and not left electrically floating. The copper backside of the TDA8357J is glued to the backside of the crystal and is *electrically connected to the ground pin (pin 5)*. The copper backside of the TDA8359J is soldered to the backside of the crystal and is *electrically connected to the ground pin (pin 5)*.

**F. Circuit**
For optimal suppression, the circuit in fig 38 can be used as guidance.

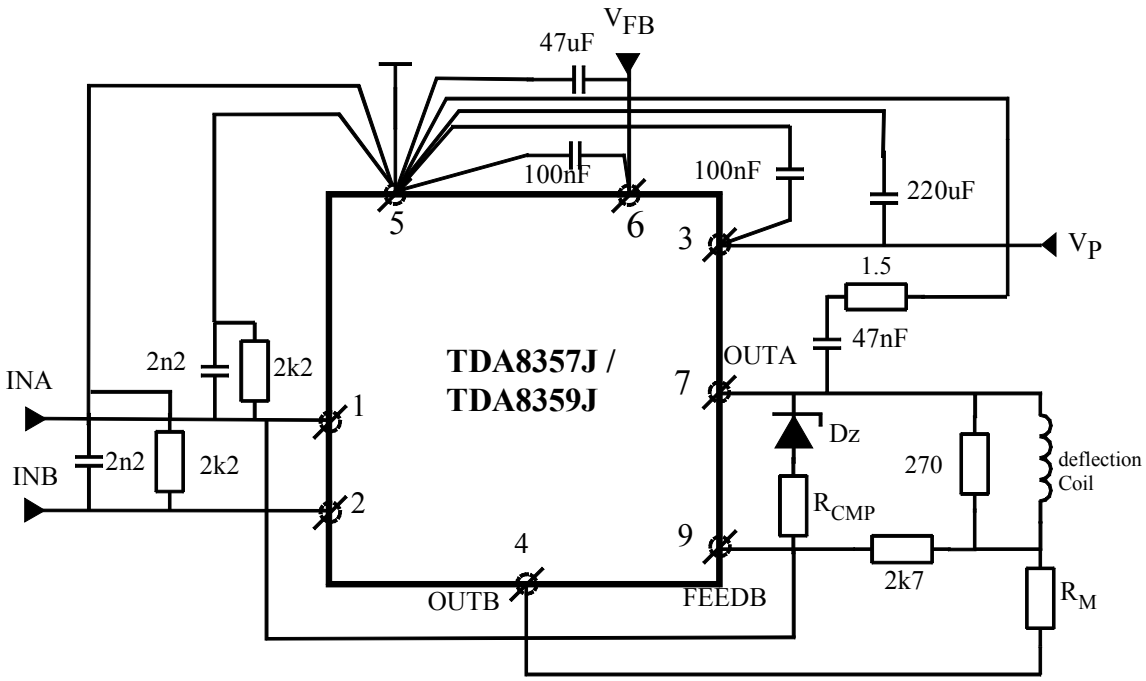



fig 38: Recommended application for optimal suppression.

### 2.19 Improved temperature coefficient in TDA8357JN2 / TDA8359JN2

The TDA8357JN2 / TDA8359JN2 have an improved temperature coefficient. A small layout modification is made in the TDA8357JN2 / TDA8359JN2, which reduces a temperature influence of the vertical amplitude. This temperature influence is checked in a customer TV-application. The picture height of the picture tube used is 410 mm. The results found are that the temperature influence of the vertical amplitude is reduced by a factor of 2. The behaviour equals our predecessor range of vertical deflection output amplifiers.

### 2.20 Vertical compressed scan with TDA8357J / TDA8359J

Vertical compressed scan is used in double window applications on 16:9 picture tubes and for the display of a 16:9 picture on a 4:3 picture tube. When vertical compressed scan is used with the TDA935X/6X/8X / TDA955X/6X/8X family (VX = 0, OSVE = 1) the black current measuring lines are written in the vertical overscan. These measuring lines are written in the vertical overscan during the last four lines of the vertical flyback period. After the last line is written the vertical drive signal jumps to the starting point of the video lines. At this moment the output signal of the TDA8357J / TDA8359J cannot follow the fast changing input signal, which forces the TDA8357J / TDA8359J into an open loop condition. See fig 39.
**This can be prevented by using a zener diode from pin 4 OUTB to pin 5 GND.** See fig 40. The zener diode prevents the output of the TDA8357J / TDA8359J to be clipped to the supply voltage. The value of the zener diode has to be between the supply voltage (about 2V lower) and the maximum output voltage on OUTB (about 1 V higher). The zener diode must have low internal resistance and must be able to consume a peak current of about 2A, to assure proper operation.

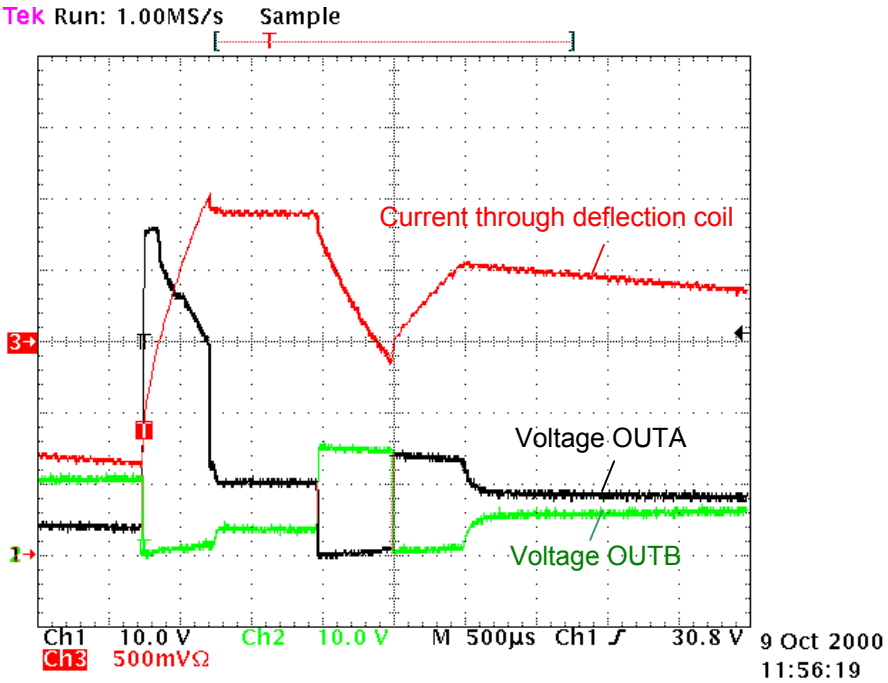



fig 39: Vertical compressed scan with TDA8357J / TDA8359J

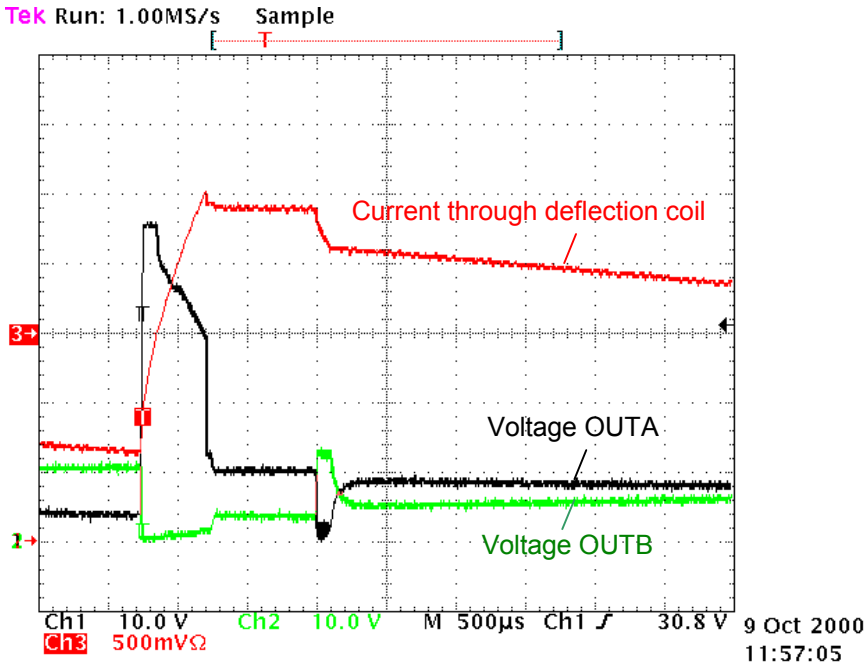



fig 40: Vertical compressed scan with TDA8357J / TDA8359J with a zener diode on pin 4 OUTB to GND

### 2.21 Application design procedure of the TDA8357J / T DA8359J.

Below is explained how to start with a design-in of the TDA8357J / TDA8359J.

For the design-in of TDA8357J / TDA8359J it is advised to use the following design steps:

1. **Start with calculating the conversion resistors $R_{CV1,2}$.** Read the typical peak to peak output current $I_{1,2(p\text{-}p)}$ and the bias output current $I_{I1,2(bias)}$ from the vertical deflection driver. Take $V_{I(bias)} + V_{I(peak)}$ <1.5V for room for vertical alignment.(max =1.6V) and take $V_{I(bias)} - V_{I(peak)} > 0.3V$ for optimum linearity

   $R_{CV}$ can be calculated by:

$$R_{CV1,2} = \frac{V_{i(bias)} + V_{i(peak)}}{I_{i1,2(bias)} + \frac{I_{i1,2(p-p)}}{2}} \text{ or } R_{CV1,2} = \frac{V_{i(bias)} - V_{i(peak)}}{I_{i1,2(bias)} - \frac{I_{i1,2(p-p)}}{2}}$$

   When a TDA884X/5X (one chip family), TDA886X/7X/8X (bocma family), TDA935X/6X/8X or TDA955X/6X/8X (ultimate one chip family) driver is used, a value of **2k2** for $R_{CV1,2}$ will do.

1. **Calculate the measuring resistor $R_M$.** Read the peak to peak value of the vertical deflection current from the picture tube coil specification. This is the edge to edge value, so overscan has to be included (about 5%).

   The measuring resistor $R_M$ can be calculated by means of the formula:

$$R_M = \frac{V_{i(dif)(p-p)}}{I_{o(p-p)}}$$

$$V_{i(dif)(p-p)} = V_{INA} - V_{INB}$$

$$V_{i(dif)(p-p)} = I_{i1(p-p)} * R_{CV1} - (-I_{i2(p-p)} * R_{CV2})$$

2. **Calculate the minimum main supply voltage $V_P$.** It should be as low as possible to avoid high dissipation. Read the DC-resistance $R_{coil(cold)}$ and inductance $L_{coil}$ of the vertical deflection coil. Read the value of $V_{loss}$ in fig 32. Determine the wanted maximum vertical frequency $f_{vert(max)}$.

   The required power supply voltage $V_P$ for the first part of the scan:

$$V_{P(1)} = \frac{I_{o(p-p)}}{2} \times \left(R_{coil(hot)} + R_M\right) - L_{coil} \times I_{o(p-p)} \times f_{vert(\max)} + V_{loss(1)}$$

   The required power supply voltage $V_P$ for the second part of the scan:

$$V_{P(2)} = \frac{I_{o(p-p)}}{2} \times \left(R_{coil(hot)} + R_M\right) + L_{coil} \times I_{o(p-p)} \times f_{vert(\max)} + V_{loss(2)}$$

Eventually, after calculating the voltage supply by means of the above formulae, the minimum required value has to be the highest of the two values $V_{P(1)}$ and $V_{P(2)}$. Eventually, this value has to be increased by 5% due to spread in the line output transformer and the deflection coil.

3. **Calculate the flyback supply voltage $V_P$.** Determine the wanted flyback time $t_{FB}$.
   The flyback supply voltage can be calculated by:

$$V_{FB} = \frac{I_{o(p-p)} \times \left(R_{coil(hot)} + R_M\right)}{1 - e^{-t_{FB}/x}}$$

   Where:

$$x = \frac{L_{coil}}{R_{coil(hot)} + R_M}$$

4. **Calculate the compensation resistor $R_{CMP}$.** Take a value of $V_{loss(FB)}$ of 8V. Read the value of the damping resistor $R_{D1}$. A value of 270Ω is recommended. Check for damping resistor on the deflection coil unit. Take the value of the zenerdiode $V_Z$ same as value of $V_p$

   The compensation resistor $R_{CMP}$ is calculated in the following way:

$$R_{CMP} = \frac{\left(V_{FB} - V_{loss(FB)} - V_Z\right) \times R_{D1} \times R_{CV1}}{\left(V_{FB} - V_{loss(FB)} - \frac{I_{o(p-p)}}{2} \times R_{coil(hot)}\right) \times R_M}$$

5. **Choose a value of $R_s$ of 2.7kΩ.**

6. **Calculate the heatsink.** . The heatsink must be chosen in such a way that the temperature of the die does not exceed the maximum allowable temperature of 150°C, as specified in the device specification. However, in general we recommend designing for an average die temperature that does not exceed **120°C.** So take a value for the die temperature of 120°C. The value of the thermal resistance between die (junction) and case $R_{th(j-c)}$ is 6 K/W for TDA8357J and is 3 K/W for TDA8359J. The value of the thermal resistance between case and heatsink $R_{th(c-h)}$ , depends on the mounting method. See table of sec. 2.15.

   The total power dissipation $P_{tot}$ is calculated by:

$$P_{tot} = P_{\sup} - P_L = \left[\frac{V_p \times I_{o(p-p)}}{4} + V_p \times 0.015 + 0.3\right] - \left[\frac{I_{o(p-p)}^2 \times \left(1.2 \times R_{coil} + R_M\right)}{12}\right]$$

   The heatsink temperature $T_h$ can be calculated: Determine the maximum ambient temperature $T_{amb(max)}$

$$T_h = T_{amb(\max)} + \left(R_{th(h-a)} \times P_{tot}\right)$$

The thermal resistance between heatsink and the ambient $R_{th(h-a)}$ can be calculated by:

$$\Leftrightarrow R_{th(h-a)} = \frac{T_j - T_{amb(\max)}}{P_{tot}} - \left(R_{th(j-c)} + R_{th(c-h)}\right)$$

7. **Connect the vertical guard.** See sec. 2.10 for a detailed description.

8. Good HF decoupling of both supplies (pin 3 and 6) is necessary. The use of a 100 nF foil or MKT capacitor (not SMD) which is mounted as close as possible to both power supply pins and to ground is strongly recommended.

9. Recommended values for the elcaps on the supplies are 220µF at pin 3 ($V_P$) and 47µF at pin 6 ($V_{FB}$).

10. For flashover or other overstress protection it is recommended to connect an RC-filter between OUTA (pin 7) and ground (pin 5) that consists of 1.5Ω in series with 47nF and should be connected as close as possible to the pins of the TDA8357J / TDA8359J.

11. Pay attention to the symmetry of the tracks to the input pins (pin 1 and 2). Long tracks should be avoided. The use of decoupling capacitors between the input pins and ground minimises the interference susceptibility. Both decoupling capacitors must have the same value and should be placed close to pin 1 and pin 2, just like the input resistors. If the value of these capacitors is too high, minor oscillations *could* occur at the start- or end of the scan. The recommended value is 2.2nF.

## 3. DIFFERENCES BETWEEN N1 AND N2

In this chapter is given a summary of the differences between TDA8357J / 59JN1 and TDA8357J / 59JN2. **No changes have to be made in the application, when changing from N1 to N2.**

### 3.1.1 Adaptive control of the flyback switch

The waveform during part B of the flyback waveform has a shape that is created by the adaptive control of the flyback switch, which operates as follows. The output current of the flyback switch is measured on a certain level onwards, the drive of the flyback switch is increased, thus lowering the impedance of the flyback switch at increasing flyback current, until it has reached a certain stable value. Now the end of the flyback has reached.

In the TDA8359JN2 / TDA8357JN2 the adaptive control circuit is activated at all values of the output current. This results in a lower dissipation in the flyback switch and a somewhat shorter flyback time. In the TDA8359JN1 / TDA8357JN1 the adaptive control circuit is not activated at a low output current. The small difference in the output voltage is given in fig 41:

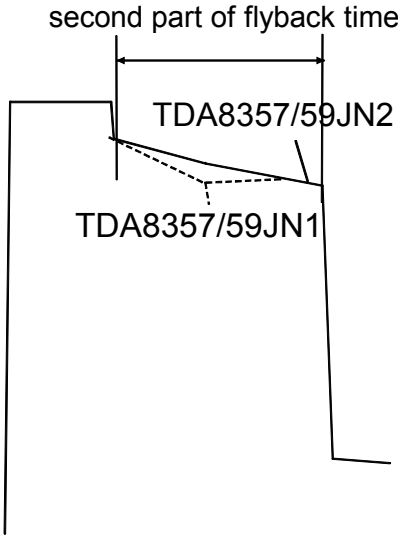



fig 41: Small difference in output voltage (flyback pulse) between N1 and N2

### 3.1.2 Flashover behaviour of TDA8357JN2 / TDA8359JN2

The TDA8357JN2 / TDA8359JN2 have improved robustness of the internal low substrate leakage current diodes against flashover by construction and a new process. Evaluation in several customer sets with only a small RC-filter (47nF + 1.5Ω) from pin 7 OUTA to pin 5 GND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during flash testing on critical pins like focus and VG2.

From our experiences with flashover and other overstress testing in the past it is recommended, see fig 42:

- HF decoupling capacitors of the supplies $V_P$ and $V_{FB}$ must be close to pins of the IC in the PCB-layout. These capacitors must be foil or MKT, not SMD.
- Grounding of all components to same ground as the IC: pin 5 GND. Avoid ground loops in the PCB-layout.

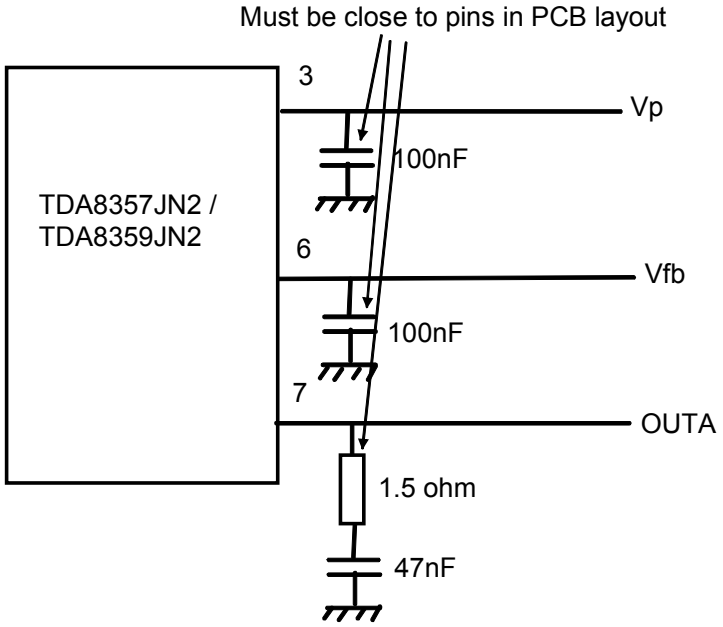



fig 42: Recommended layout for flashover protection

### 3.2 ESD-gun test

Next to the standard ESD-test on the TDA8357J / TDA8359J (Human Body Model and Machine Model), another ESD-test is introduced by some customers. This ESD-test is introduced to test the application, which the TDA8357J / TDA8359J is used in. This ESD-test is carried out by a standard ESD-gun (NSG 435), which is discharged on the connections of the vertical deflection coil mounted on the neck of the picture tube. The standard ESD-gun is discharged with a capacity of 150 pF and a series resistor of 330 Ω. This capacitor and resistor are standard IEC1000-4-2 (IEC 801-2, 1991) and are inside of the ESD-gun.

With the TDA8357JN1 / TDA8359JN1, some external components were needed for a better ESD-gun test behaviour. The TDA8357JN2 / TDA8359JN2 have improved robustness of internal low substrate leakage current diodes against overstress behaviour by construction and a new process. Evaluation in several customer sets with only a small RC-filter (47nF + 1.5Ω) from pin 7 OUTA to pin 5 GND and without any other external protections (coils, diodes and zenerdiodes) resulted in **no failures** during ESD-gun testing up till 16.5 kV air discharge.

From our experiences with ESD-gun testing in the past it is recommended:

- HF decoupling capacitors of the supplies $V_P$ and $V_{FB}$ must be close to pins of the IC in the PCB-layout. When the HF decoupling capacitor of the flyback supply $V_{FB}$ is not close to the pin $V_{FB}$, the robustness is much lower. These capacitors must be foil or MKT, not SMD.

- Grounding of all components to same ground as the IC: pin 5 GND. Avoid ground loops in the PCB-layout.

### 3.3 Improved temperature coefficient in TDA8357JN2 / TDA8359JN2

The TDA8357JN2 / TDA8359JN2 have an improved temperature coefficient. A small layout modification is made in the TDA8357JN2 / TDA8359JN2, which reduces a temperature influence of the vertical amplitude. This temperature influence is checked in a customer TV-application. The picture height of the picture tube used is 410 mm. The results found are that the temperature influence of the vertical amplitude is reduced by a factor of 2. The behaviour equals our predecessor range of vertical deflection output amplifiers.

# 4. EXTENDED APPLICATION INVESTIGATION

## 4.1 Introduction

A more detailed investigation may be required, depending on the application. Whether such an investigation is necessary can be determined by comparing the actual application with the figures in the next sections.

## 4.2 Current peak at the end of flyback time.

For flashover or other overstress protection it is recommended to connect a RC-filter between OUTA (pin 7) and ground (pin 5) that consists of 1.5Ω in series with 47nF and should be connected as close as possible to the pins of the TDA8357J / TDA8359J.

When an RC-filter is used between OUTA and GND in an application with the TDA8357J / TDA8359J, a small current peak at the end of the flyback time arises. In the next case one can see that these current peaks *don't damage* the TDA8357J / TDA8359J.

### 4.2.1 Application without RC-filter.

In fig 43 the voltage of OUTA (pin 7), the current of OUTA (pin 7) and the current of GND (pin 5) is measured in an application *without* RC-filter

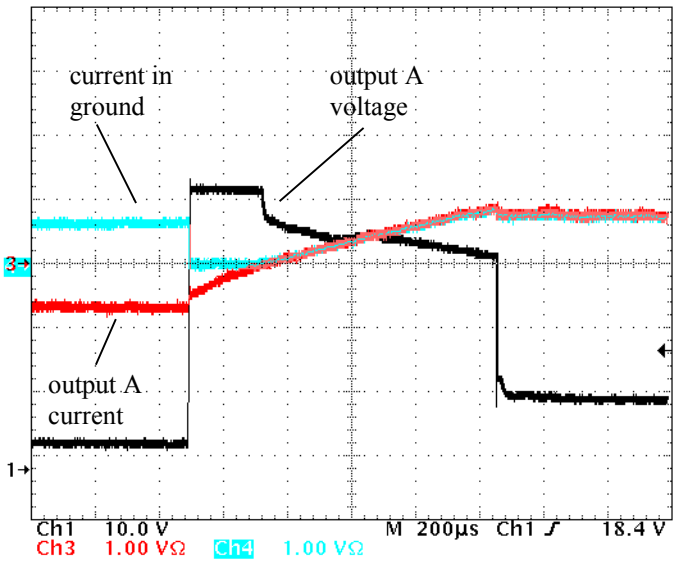



fig 43: Flyback time of application without RC-filter on OUTA

In fig 44 is the beginning of the flyback stretched out and in fig 45 the end of the flyback is stretched out.

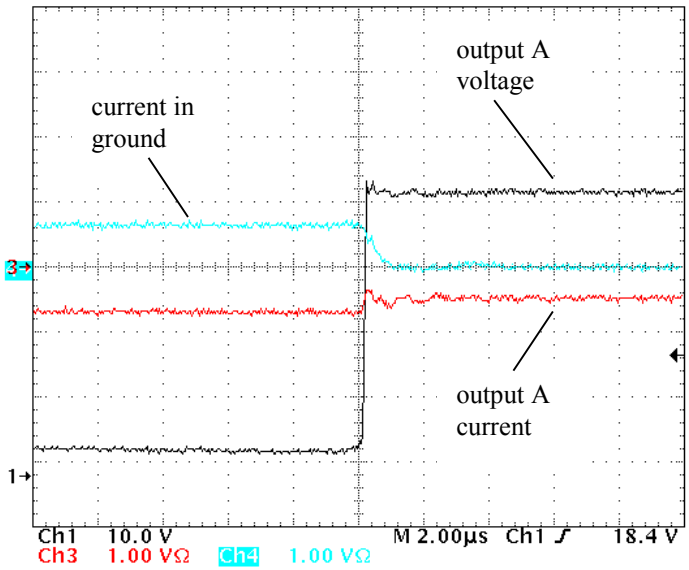



fig 44: Flyback time of application without RC-filter on OUTA.

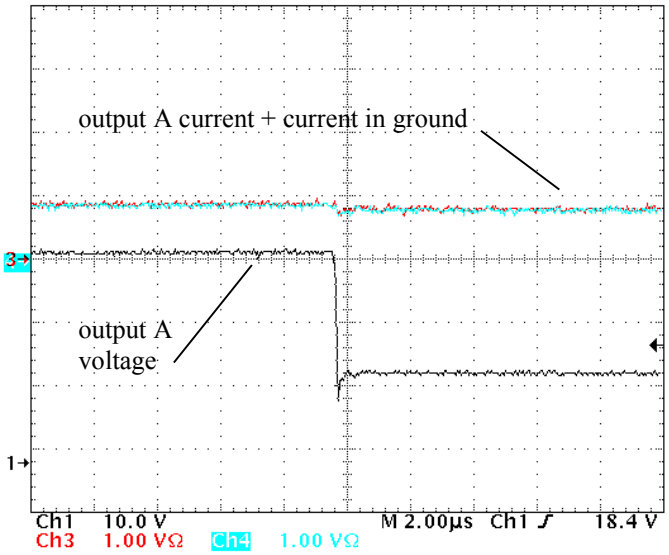



fig 45: Flyback time of application without RC-filter on OUTA.

As can be seen in fig 44 and in fig 45, there are no current peaks at output A or ground at the start- and end of the flyback. The small step in the output A current is the current that flows through the damping resistor.

### 4.2.2 Application with RC-filter 47 nF + 1.5 Ohm

When a low ohmic RC-filter (47 nF + 1.5 Ohm) is used between OUTA and ground for flash protection, a peak current occurs at OUTA and GND at the end of the flyback. See fig 46 and fig 47.

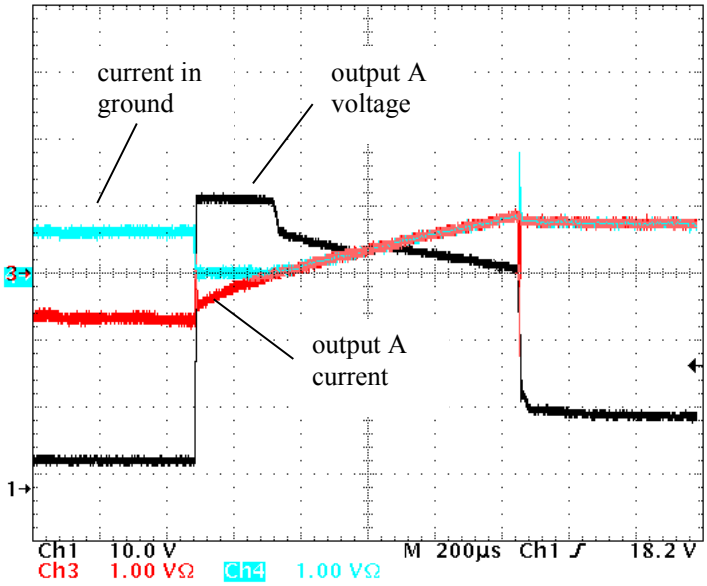



fig 46: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

In fig 47 the beginning of the flyback is stretched out and in fig 48 the end of the flyback is stretched out.

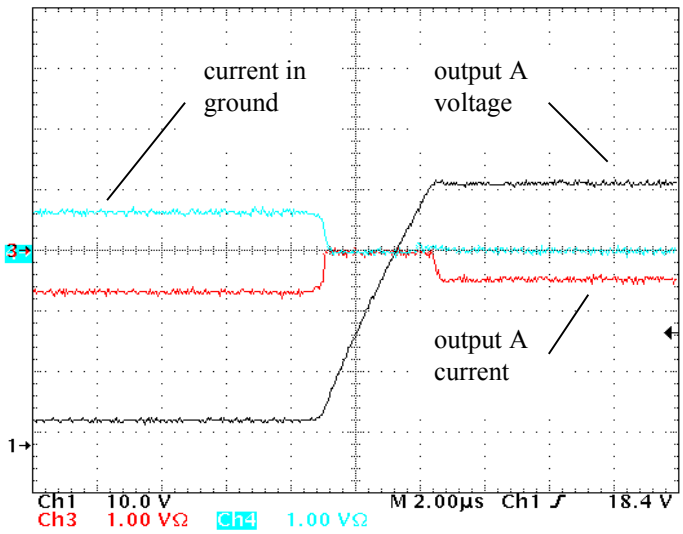



fig 47: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

As can be seen in fig 47 the rise time of the flyback pulse increases when an RC-filter on OUTA is used. This has no influence on the performance of the TDA8357J / TDA8359J. During the rise time of the flyback, the current of pin OUTA is zero. This is due to charging the capacitor of the RC-filter. Then the current from the deflection coil flows in the capacitor of the RC-filter.

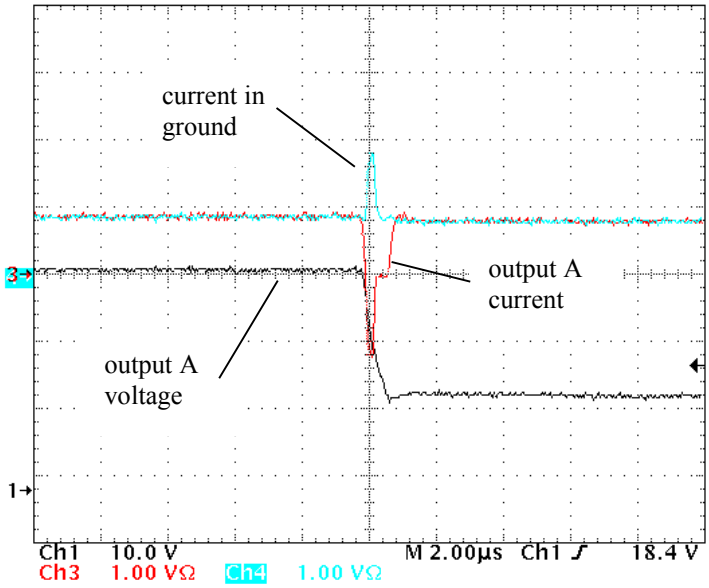



fig 48: Application with RC-filter between OUTA and ground (47 nF + 1.5 Ohm).

As can be seen in fig 48 a current peak of 1.8 A occurs in the GND pin at the end of the flyback. Also a negative current peak of 1.2 A occurs in the OUTA at the end of the flyback. These peaks are due to discharge of the capacitor of the RC-filter. The discharge current of the capacitor flows via the bottom transistor of the A-output of TDA8357J / TDA8359J to GND. See fig 49. Because the time of these peaks is *very short*, this will cause *no damage* to the TDA8357J / TDA8359J.

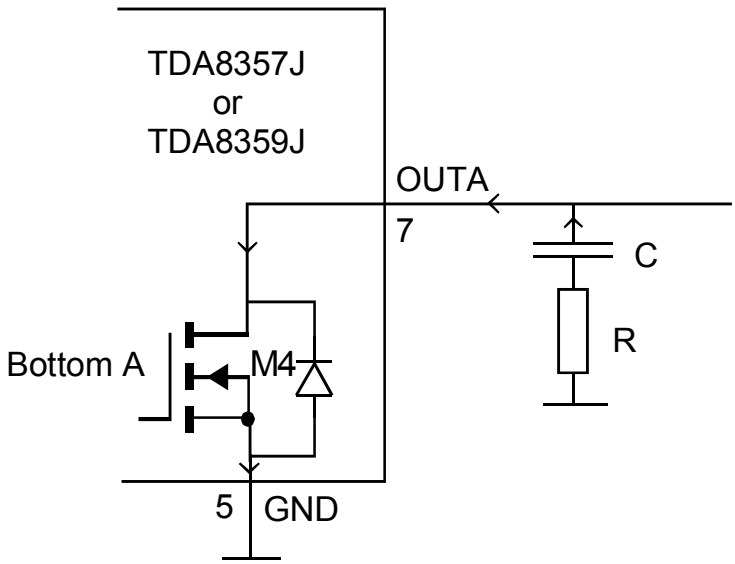



fig 49: TDA8357J / TDA8359J, current flow when discharging C.

# 5. APPENDIX

## 5.1 Calculating the power $P_{sup}$

The power that is delivered by the supply is calculated in the following way:

The current ($I_{sup}$) that is delivered by the power supply during the scan time is illustrated in the figure below.

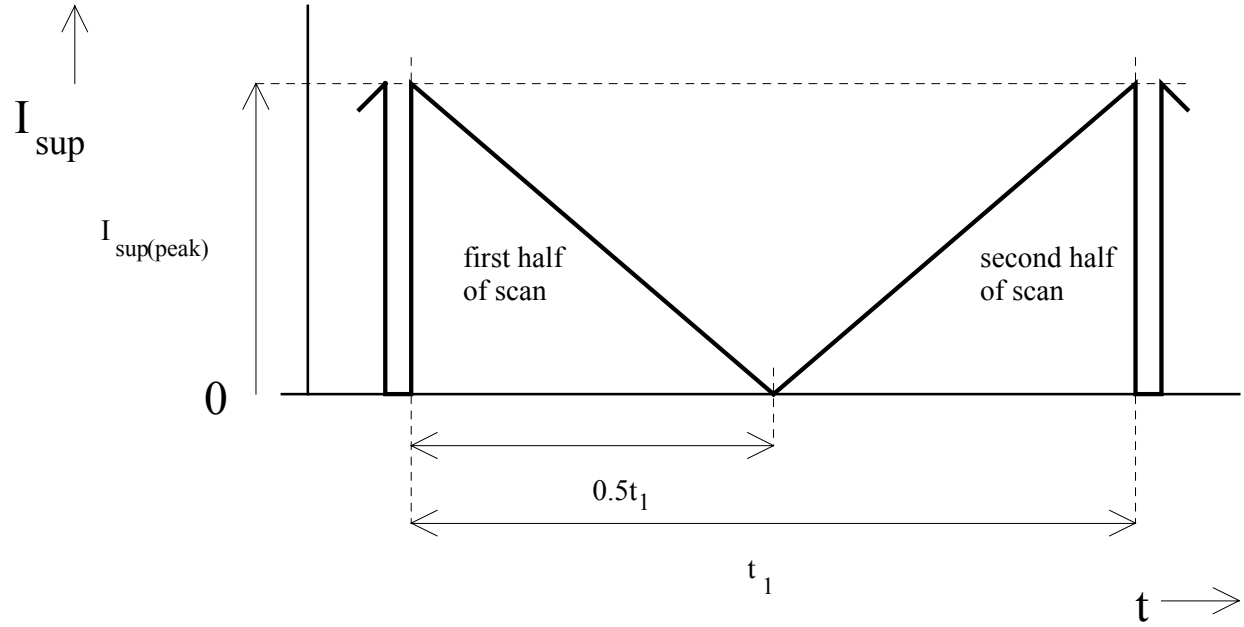



fig 50: Current of the supply.

The *momentary* supply current $I_{sup}$ is expressed by the formula:

for $0 \le t \le 0.5t_1$ (first half of the scan):

$$I_{\sup}(t) = I_{\sup(peak)} - \left(2 \times I_{\sup(peak)} \times \frac{t}{t_1}\right)$$

$$\Leftrightarrow I_{\sup}(t) = I_{\sup(peak)} \times \left(1 - 2 \times \frac{t}{t_1}\right)$$

for $0.5t \le t \le t_1$ (second half of the scan):

$$I_{\sup}(t) = \left(2 \times I_{\sup(peak)} \times \frac{t}{t_1}\right) - I_{\sup(peak)}$$

$$\Leftrightarrow I_{\sup}(t) = I_{\sup(peak)} \times \left(2 \times \frac{t}{t_1} - 1\right)$$

Because of the symmetry for the first- and the second half of the power supply, the *average* power delivered by the supply is:

$$P_{sup} = 2 \times \frac{1}{t_1} \times \int_0^{0.5t_1} \left( V_P \times I_{sup} - 2 \times V_p \times I_{sup} \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{sup} = \frac{2}{t_1} \times \int_0^{0.5t_1} V_P \times I_{sup} \times \left( 1 - 2 \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{sup} = \frac{2 \times V_P \times I_{sup}}{t_1} \times \int_0^{0.5t_1} \left( 1 - 2 \times \frac{t}{t_1} \right) dt$$

$$\Leftrightarrow P_{sup} = \frac{2 \times V_P \times I_{sup}}{t_1} \times \left[ t - \frac{t^2}{t_1} \right]_0^{0.5t_1}$$

$$\Leftrightarrow P_{sup} = \frac{2 \times V_P \times I_{sup}}{t_1} \times \frac{1}{4} \times t_1$$

$$\Leftrightarrow P_{sup} = \frac{V_P \times I_{sup}}{2}$$

or $P_{sup} = \frac{V_P \times I_{o(p-p)}}{4}$ because $I_{sup} = I_{o(p-p)}$

### 5.2 Calculating the power dissipation $P_L$

The power dissipation in the load ($R_{coil}$ + $R_M$) is calculated in the following way:

The current through the deflection coil $I_o$ and the current through the measurement resistor $R_M$ are equal and can be seen in fig 51.

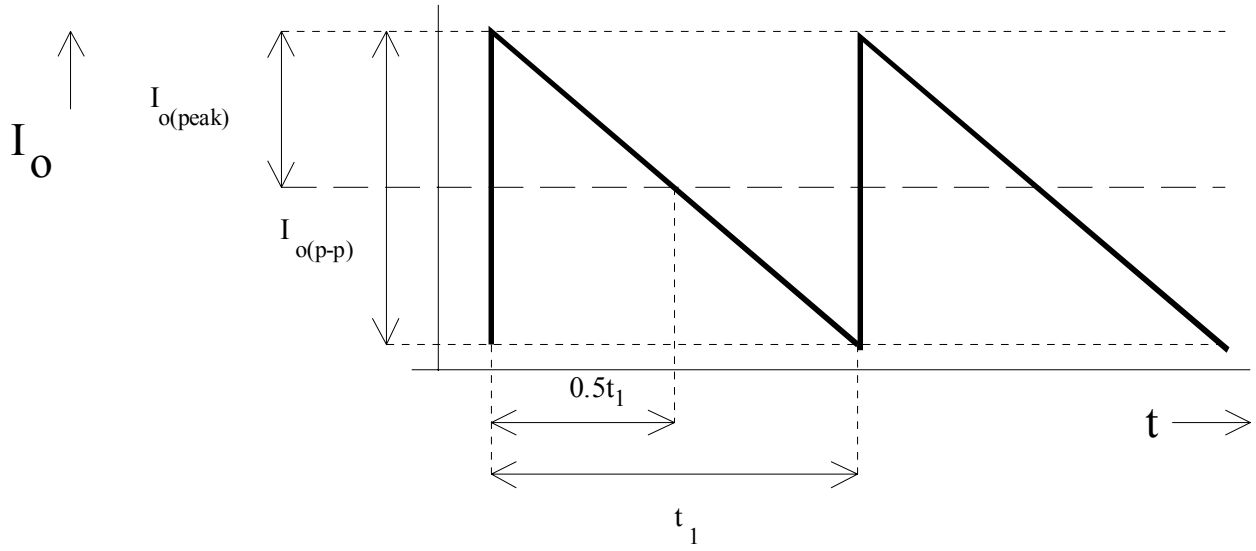



fig 51: Current through the deflection coil and $R_M$.

The *momentary* current in the deflection coil is given by:

$$I_o(t) = I_{o(peak)} - \left(2 \times I_{o(peak)} \times \frac{t}{t_1}\right)$$

$$\Leftrightarrow I_o(t) = I_{o(peak)} \times \left(1 - 2 \times \frac{t}{t_1}\right)$$

The *momentary* dissipated power $P_L(t)$ in the load ($R_{coil}$ + $R_M$):

since: $P = I^2 \times R$

$$\Leftrightarrow P_L(t) = I_{o(peak)}{}^2 \times \left(1 - 2 \times \frac{t}{t_1}\right)^2 \times (R_{coil} + R_M)$$

Because of the symmetry of the first- and the second half of the current through the load, the *average* power dissipation in the load is:

$$P_L = \frac{2}{t_1} \times \int_0^{0.5t_1} \left(I_{o(peak)}\right)^2 \times \left(1 - 2 \times \frac{t}{t_1}\right)^2 \times \left(R_{coil} + R_M\right) dt$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{o(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \int_0^{0.5t_1} \left(1 - 2 \times \frac{t}{t_1}\right)^2 dt$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{o(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \int_0^{0.5t_1} \left(1 - 4 \times \frac{t}{t_1} + 4\frac{t^2}{t_1^2}\right) dt$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{coil(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \left[t - \frac{4}{2} \cdot \frac{t^2}{t_1} + \frac{4}{3} \cdot \frac{t^3}{t_1^2}\right]_0^{0.5t_1}$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{o(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \left[0.5 \cdot t_1 - 2 \cdot \frac{\left(0.5 \cdot t_1\right)^2}{t_1} + \frac{4}{3} \cdot \frac{\left(0.5 \cdot t_1\right)^3}{t_1^2}\right]$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{o(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \left[\frac{1}{2} \cdot t_1 - \frac{1}{2} \cdot t_1 + \frac{1}{6} \cdot t_1\right]$$

$$\Leftrightarrow P_L = \frac{2 \times \left(I_{o(peak)}\right)^2 \times \left(R_{coil} + R_M\right)}{t_1} \times \frac{1}{6} \cdot t_1$$

$$\Leftrightarrow P_L = \frac{I_{o(peak)}{}^2 \times \left(R_{coil} + R_M\right)}{3}$$

or $$P_L = \frac{I_{o(p-p)}{}^2 \times \left(R_{coil} + R_M\right)}{12}$$ because $$I_{o(p-p)} = 2 \times I_{o(peak)}$$

For calculations the coil resistance is multiplied by 1.2 for hot conditions of the deflection coil

$$P_L = \frac{I_{o(peak)}^2 \times (1.2 \times R_{coil} + R_M)}{3}$$

or $$P_L = \frac{I_{o(p-p)}^2 \times (1.2 \times R_{coil} + R_M)}{12}$$

## 6. REFERENCES


- Application note TDA8359JN1 (AN00039)
- Application note TDA8357JN1 (AN00016)
- Application note TDA8358JN1 (AN99009)
- Application note TDA935X/6X/8X (AN98093)
- Application note TDA884X/885X (AN98002)

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